

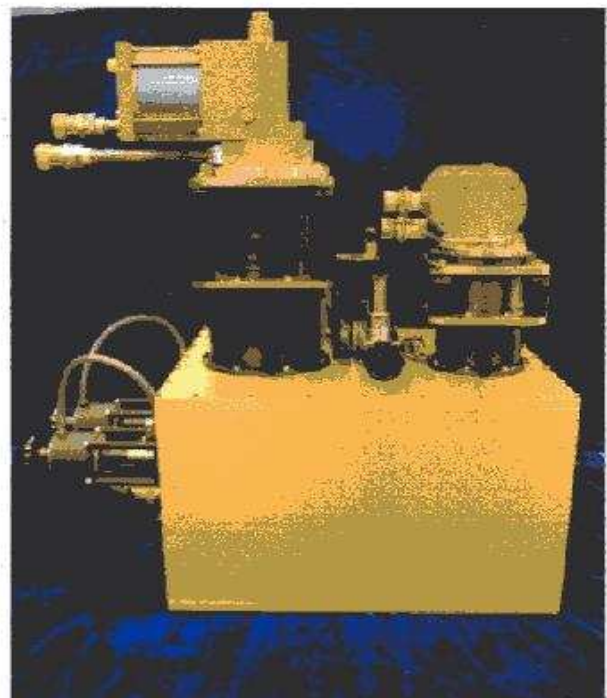
Manual de la cámara  
infrarroja doble (CID)  
proporcionado por IRLabs.  
(Primera parte)

Recopilado por Loiret  
Alejandría Dosal Trujillo.

Julio 3 de 2003.











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# Dewar Description



# **Universidad Nacional Autonoma de Mexico (U.N.A.M.)**

## **BiB Camera & InSb Camera/Spectrometer**

### **User Manual for Dewar 2977**

#### **1. Unpacking Instructions**

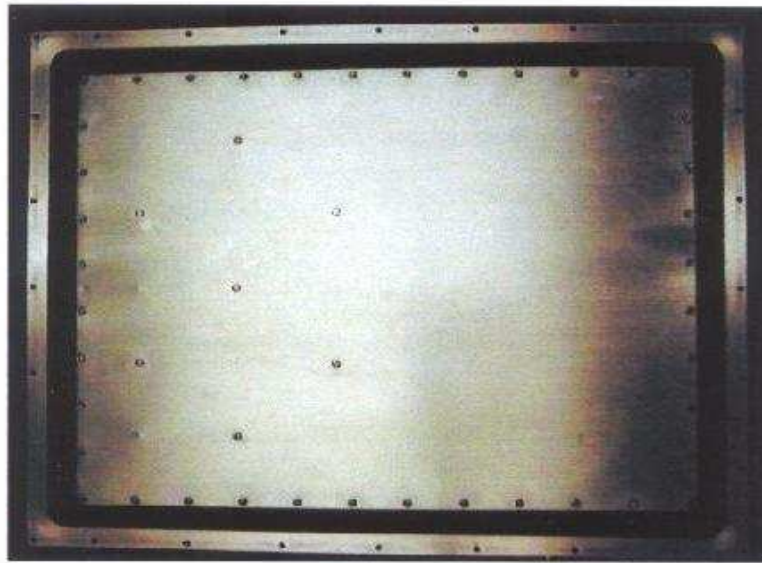
The dewar has been shipped under vacuum. This is done in order to increase the performance of the activated charcoal, giving a better vacuum. Because the charcoal is somewhat sensitive to atmospheric conditions, some simple precautions should be taken to ensure good performance.

- (1) Even when not in use, store the dewar with the guard vacuum still intact. This ensures both cleanliness and a moisture-free environment inside.
- (2) When the dewar must be opened for installation of detectors, wiring, etc., keep the amount of time that the charcoal is exposed to atmospheric pressure to a minimum.
- (3) Periodically attach the dewar to a high vacuum pump and re-evacuate the guard vacuum, as outgassing may occur over time.

The system has been carefully packed for shipment in a solid, wood shipping crate. The dewar is extremely heavy and necessitates care when removing it from the container. Once the dewar has been removed from the crate, rest it on its flat bottom plate on a suitable clean surface. Remove all protective tape and packing around the motors and dewar case. Check for any apparent shipping damage. The following steps describe the procedure Infrared Laboratories used to access the internal optical compartments. It is recommended that the user inspect the interior for any shipping damage.

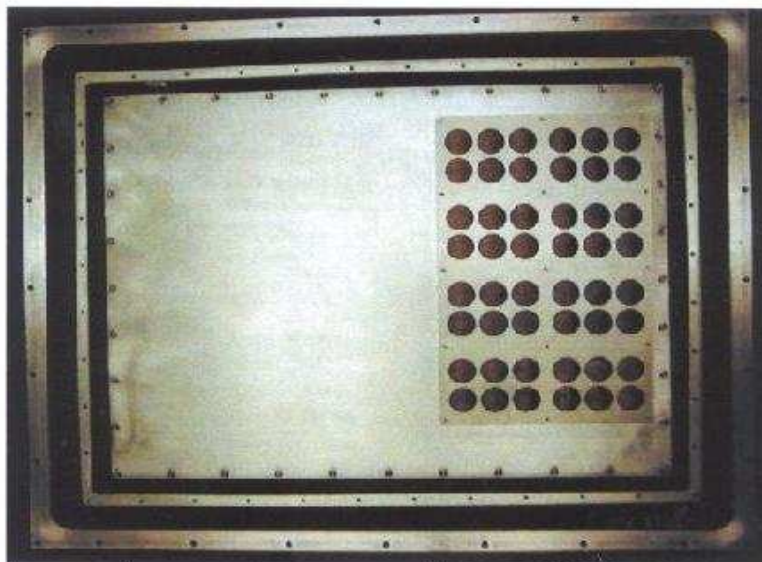
- (1) With the dewar sitting on the bottom plate, SLOWLY open the valve to release the guard vacuum.
- (2) Remove the valve by unscrewing the four (4) 8-32 socket head cap screws at its base. This step was necessary (at Infrared Labs) because the stand we used rested the dewar along the long axis where the valve protruded out and got in the way.

- (3) Turn the dewar up-side-down so that the bottom plate is facing up. Remove the twenty-eight (28) 8-32 socket head case screws around the border of the bottom plate, see Figure 1-1.



**Figure 1-1: Outer Radiation Shield Lid**

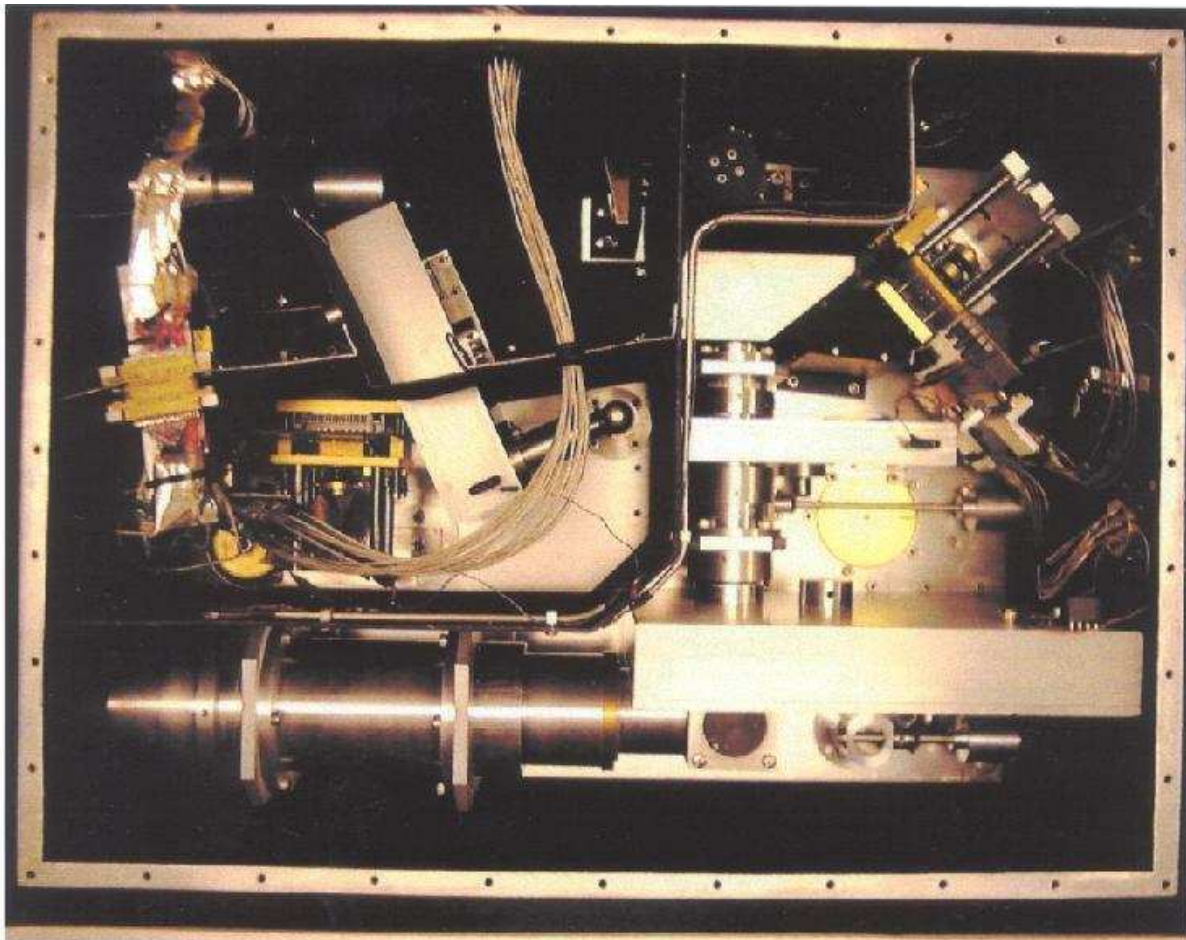
- (4) Remove the thirty-eight (38) 4-40 socket head cap screws around the periphery of the outer radiation shield lid. Do not remove the other screws in the lid, see Figure 1-2.



**Figure 1-2: Inner Radiation Shield Lid**

- (5) Remove the thirty-six (36) 4-40 socket head cap screws around the periphery of the inner radiation shield lid. Note the orientation of the shield lid. The charcoal getter box is located furthest away from the windows, see Figure 1-3.





**Figure 1-3: BiB and InSb Cameras**

With the bottom plate and radiation shield lids removed, carefully inspect the cold work surface and radiation shields for any apparent shipping damage. Both cameras are now accessible for installation of filters and apertures. See Section 3 'Installation of Optical Elements' for specific instructions. If any problems arise with the unpacking of your dewar system, do not hesitate to call Infrared Laboratories, Inc. at (520) 622-7074.

## **2. Disassembly Instructions**

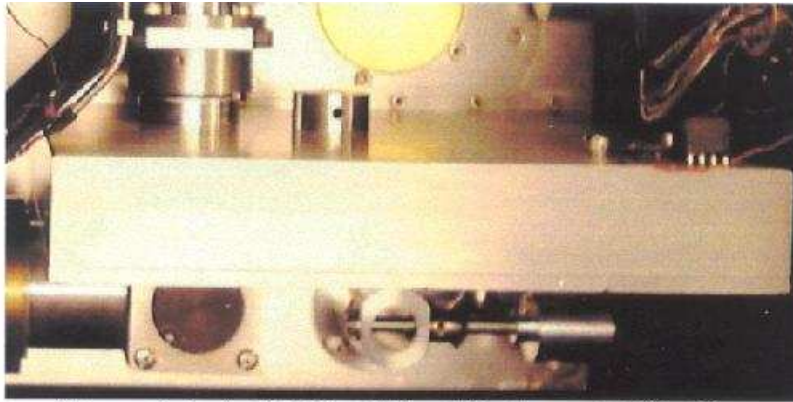
The following steps describe the disassembly of the cameras to access the filter wheels, aperture wheel, Lyot stops and array mounts and to prepare the camera for normal use.

**Caution:** Make sure you are properly grounded to avoid static charges.

### **InSb Filter Wheel Enclosure:**

- (1) Loosen the 0-80 set screw on the light tight baffle ring between the Enclosure and the second collimator optics tube. Slide it away from the filter box. See Figure 2-1.





**Figure 2-1: InSb Filter Wheel Enclosure Baffle Ring**

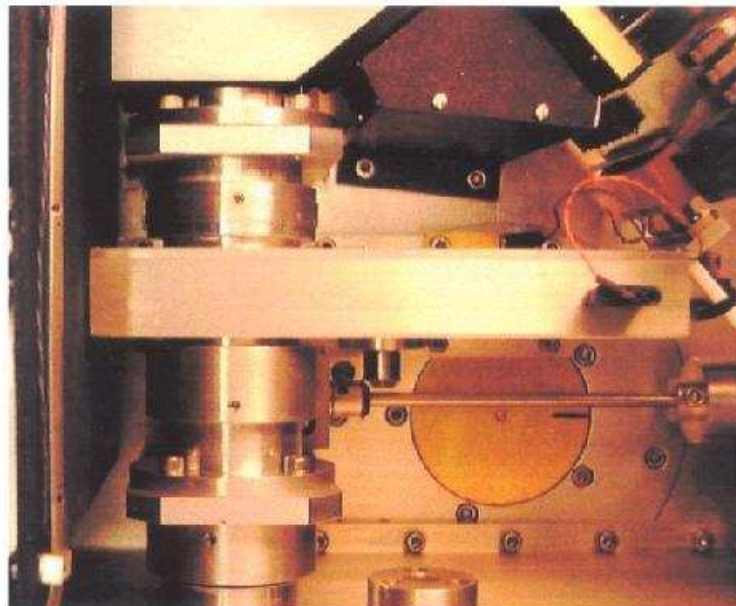
Do not forget to remove the four pin SIP connector for the Home switch and the two pin SIP connector for the temperature sensor. The connectors are wired in such a way that they can be reinstalled in either direction.

Remove the nine (9) 4-40 socket head cap screws around the base of the Enclosure. The box can now be removed from the dewar.

#### **InSb Aperture Wheel Enclosure:**

The InSb Aperture Wheel Enclosure is more difficult to remove. It can not be extracted by simply removing the base screws. The gear shaft is coupled to the outer radiation shield heat sink. It must be removed before the Enclosure can be extracted.

Loosen the two 0-80 set screws on the light tight baffle rings on either side of the Enclosure. Slide the rings away from the box. See Figure 2-2.



**Figure 2-2: InSb Aperture Wheel Enclosure Baffle Rings**

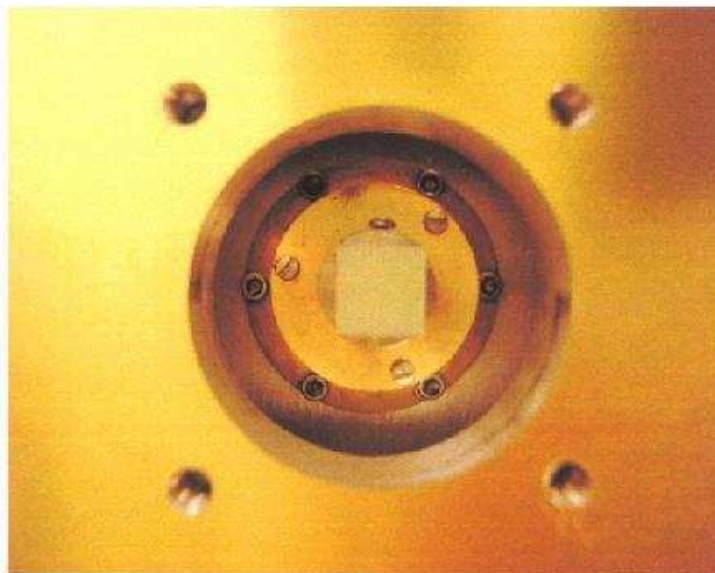
- (2) Remove the seven (7) 4-40 socket head cap screws from the base of the Enclosure. Also, loosen the 6-32 socket head set screw on the baffle cap located on the gear shaft (middle-right of Figure 2-2). Slide the baffle cap toward the gears.

Do not forget to remove the four pin SIP connector for the Home switch. The two pin SIP connector for the temperature sensor does not have to be removed. The entire sensor will be removed when the screw is unfastened. The connectors are wired in such a way that they can be reinstalled in either direction.

- (4) The gearing for the Enclosure is located under the second collimator optics tube. The collimator bracket must be removed to make room for the gears. Remove the two (2) 6-32 socket head cap screws at the foot of the bracket. The screw holes are tightly toleranced and provide adequate repeatability. Additionally, two fixed dowel pins can be inserted in the foot for added repeatability of removal. The Enclosure can freely move inside the dewar but can not be extracted.

Remove the four (4) M-4 socket head cap screws that mount the motor assembly marked '2' to the dewar case.

**Notice:** The Oldham coupler (G-10 block) mounted on the heat sink inside the recess of the dewar case (see Figure 2-3) must have a specific orientation with respect to the stainless steel 'C' bracket on the motor drive shaft. The bracket must be oriented 90 degrees to the identical 'C' bracket under the G-10 block. If the brackets are coupled in line to one another, they may bind and damage the mechanism as the shield cools.



**Figure 2-3:** Heat Sink on Outer Radiation Shield, Oldham Coupler Style



- (5) Carefully remove the six (6) 2-56 socket head cap screws around the edge of the heat sink. A pair of angled tweezers will aid in extracting each screw as it is loosened. If a screw should fall down into the case, the dewar must be lifted up-side-down and the screw should fall out.

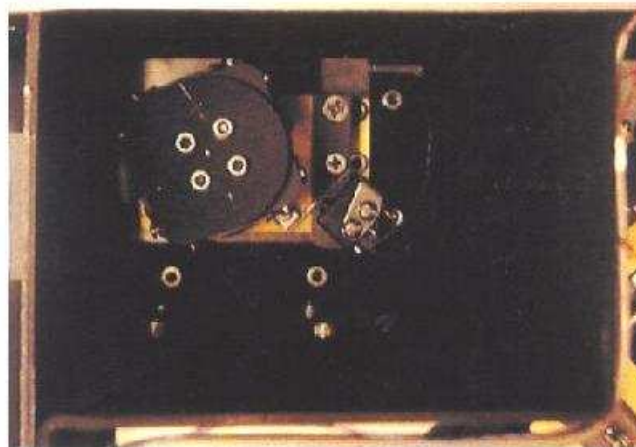
**Notice:** In Figure 2-3, the heat sink is not centered in the dewar case hole. As the dewar cools, the outer radiation shield will contract a few millimeters and center the heat sink. It is for that reason that the G-10 block (in the center) moves freely inside the 'C' brackets.

- (6) Once the heat sink has been removed, the Aperture Wheel Enclosure can be extracted by lifting the box at an angle so that the Kel-F coupler inside the baffle tube of the inner radiation shield is dislodged. The box will scrape against the baffle wall as it is removed. Care must be taken not to bend the gear shaft.

#### **InSb Grating Turret:**

The InSb grating turret is the most difficult assembly to remove from the dewar. It is housed in its own small compartment and is coupled to a heat sink (similar to the InSb Aperture Enclosure). The following describe the steps necessary to extract the turret.

- (1) Remove the four (4) 4-40 socket head cap screws at the base of the turret.
- (2) Remove the 2-56 & 4-40 Phillips flathead screws from the Home switch support bracket. To facilitate ease of reinstallation, disconnect the two pin SIP connector located at the top of the baffle wall, see upper right of Figure 2-4. The wiring can be loosened such that the Home switch can be extracted out of the compartment. The bracket can then be reinstalled to the turret easily. Finally, the entire assembly can be lowered back into the compartment.



**Figure 2-4: Turret Compartment**

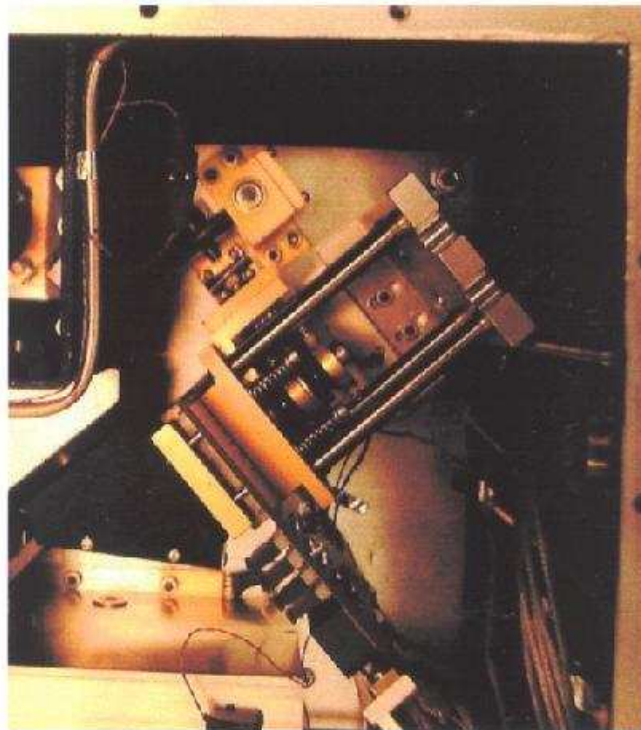


- (3) Repeat Steps 4 & 5 from 'InSb Aperture Wheel Enclosure' and remove the motor labeled '1'. Once the heat sink is removed, the turret is free to move inside its compartment.
- (4) Using a pair of large tweezers, grasp the turret and move it away from the inner radiation shield. The Kel-F coupler inside the baffle tube should dislodge and the turret can be extracted straight up.

#### **InSb Array Mount:**

**Caution:** Make sure you are properly grounded to avoid static charges.

- (1) Open the heat switch.
- (2) Remove the three (3) 4-40 socket head cap screws from the base of the array mount, see Figure 2-5.



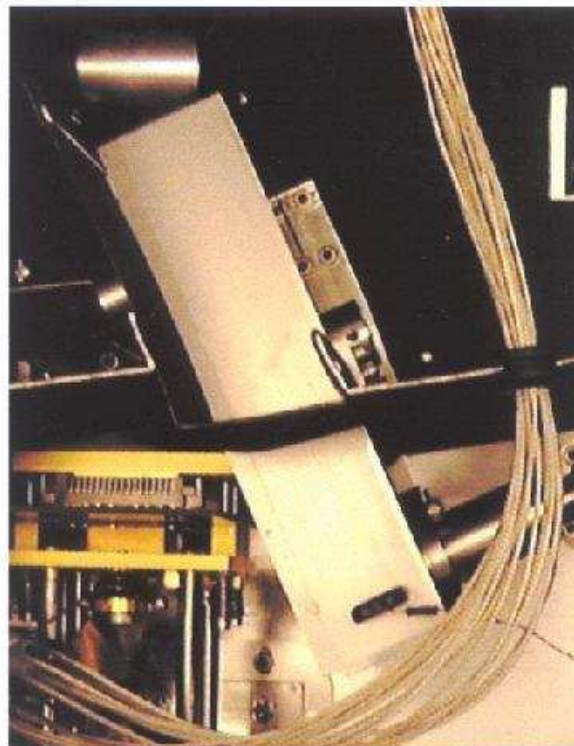
**Figure 2-5: InSb Array Mount**

Disconnect the two cables from the fanout board.

The array mount can now be removed. The front array baffle rests inside the baffle enclosure surrounding the final folding mirror. To remove the array mount, tilt it back, then straight up. Note that the position of the mount is fixed by a small bracket at the base. To reinstall the mount, simply press it against the bracket and tighten the 4-40 screws.

### **BiB Filter Wheel Enclosure:**

- (1) Remove the baffle wall above the Enclosure by sliding it straight up. Notice its orientation for reinstallation, see Figure 2-6.



**Figure 2-6: BiB Filter Wheel Enclosure**

Remove the six (6) 4-40 socket head cap screws at the base of the Enclosure. Also remove the four pin SIP connector for the Home switch.

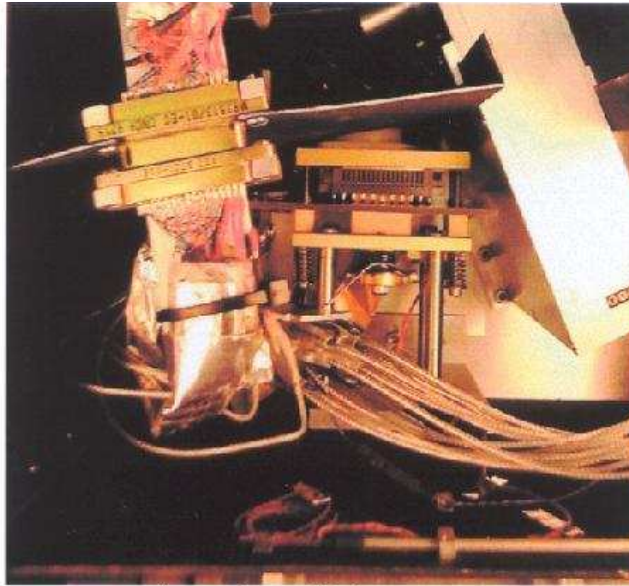
The Enclosure is coupled to the baffle walls by light tight rails. Slide the Enclosure straight up; it may be necessary to move the coax cable bundle out of the way.

### **BiB Array Mount:**

**Caution:** Make sure you are properly grounded to avoid static charges.

- (1) Remove the two (2) 4-40 socket head cap screws from the base of the array mount, see Figure 2-7.

Disconnect the two cables. One connector is located on the top of the baffle wall. The other connector is on the fanout board.



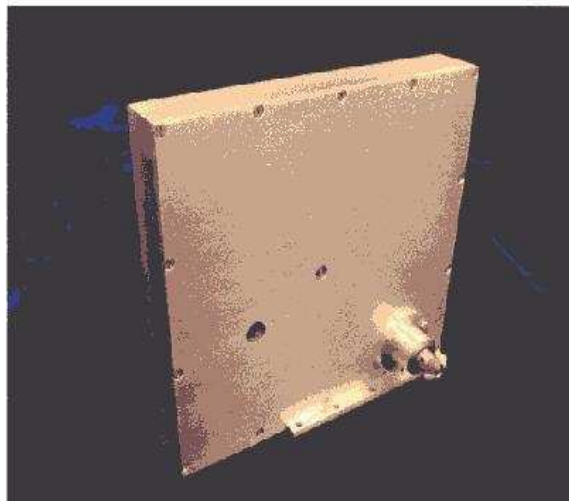
**Figure 2-7: BiB Array Mount**

- (5) The array mount can now be removed. The front array baffle rests inside the baffle wall. To remove the array mount, tilt it back, then straight up. Note that the position of the mount is fixed by a small bracket at the base. To reinstall the mount, simply press it against the bracket and tighten the 4-40 screws.

### **3. Mounting of Optical Elements**

Once the dewar has been fully disassembled, access to the filter wheels and aperture wheel can be performed.

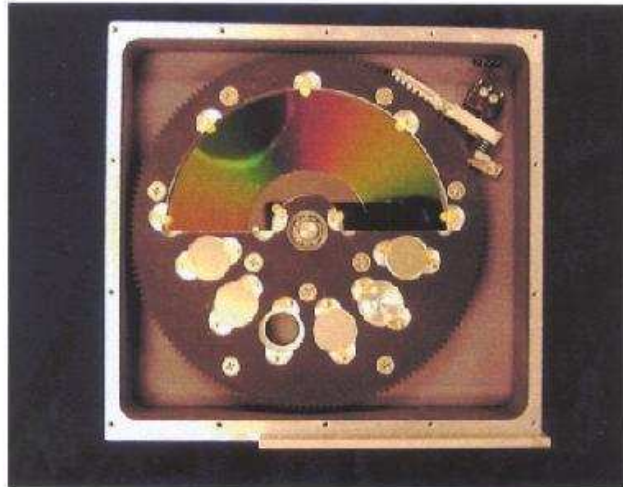
**InSb Filter Wheel:**



**Figure 3-1: InSb Filter Wheel Enclosure**



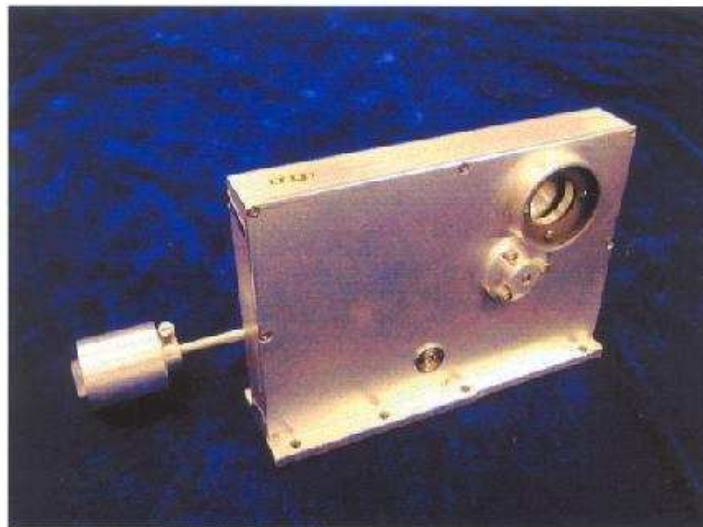
- (1) Set the InSb Filter Wheel Enclosure on a flat, clean surface with the gear pointing up.
- (2) Remove the fourteen (14) 2-56 flat head Phillips screws around the cover plate.
- (3) The cover plate is spring loaded. Apply pressure to the center of the plate while prying the edges open. Once the press fit rod in the center is detached, the plate can be removed, see Figure 3-2.



**Figure 3-2: Inside the InSb Filter Wheel Enclosure**

- (4) Each filter is secured in its recess by two clips. To install or replace a filter, loosen the two clips and rotate them aside.

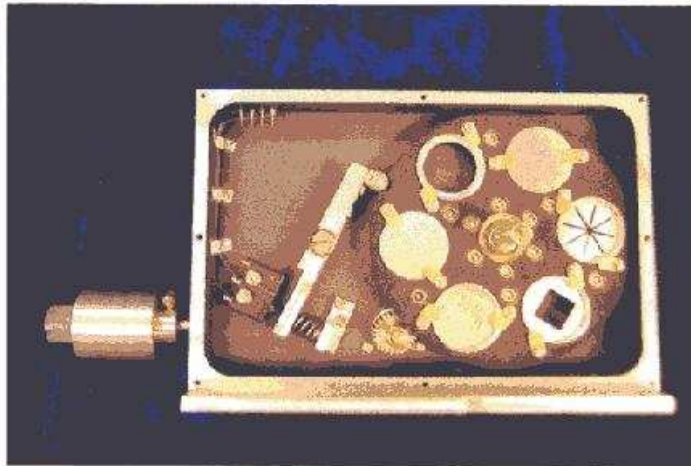
#### **InSb Aperture Wheel:**



**Figure 3-3: InSb Aperture Wheel Enclosure**

- (1) Remove the eight (8) 2-56 flat head Phillips screws around the cover plate.

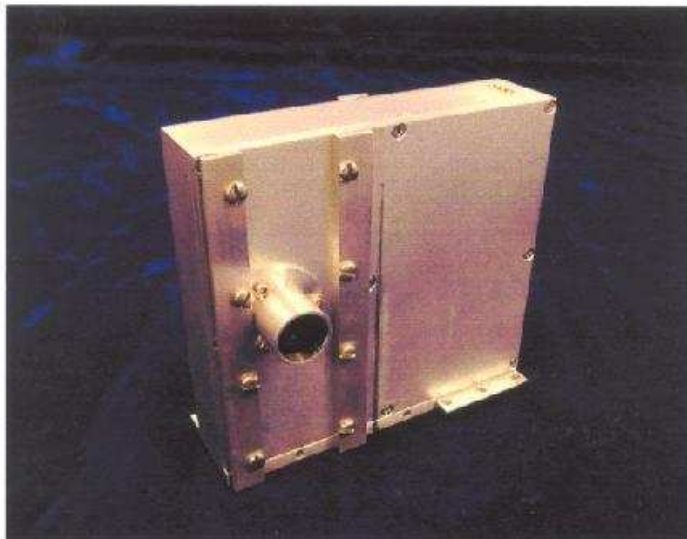
The cover plate is spring loaded. Apply pressure to the center of the plate while prying the edges open. Once the press fit rod in the center is detached, the plate can be removed, see Figure 3-4.



**Figure 3-4: Inside the InSb Aperture Wheel Enclosure**

Each filter is secured in its recess by two clips. To install or replace a filter, loosen the two clips and rotate them aside.

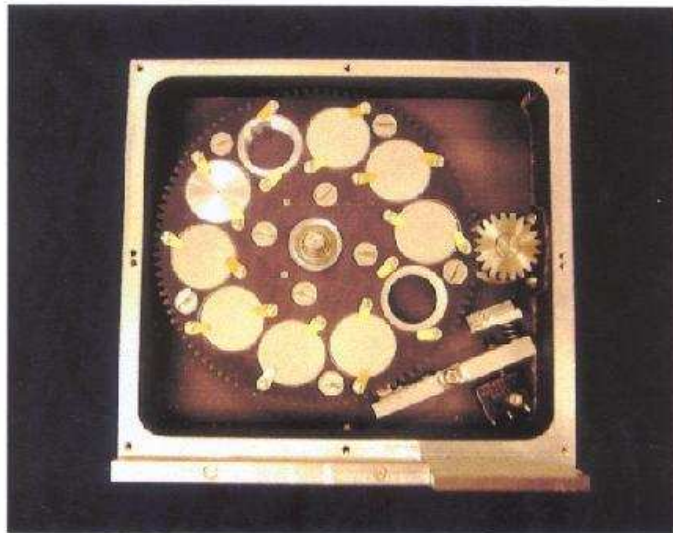
**BiB Filter Wheel:**



**Figure 3-5: BiB Filter Wheel Enclosure**

Remove the right rail bracket by unscrewing the four (4) 4-40 pan head slotted screws, see Figure 3-5.

- (2) Remove the eight (8) 2-56 flat head Phillips screws around the cover plate.
- (4) The cover plate is spring loaded. Apply pressure to the center of the plate while prying the edges open. Once the press fit rod in the center is detached, the plate can be removed, see Figure 3-6.



**Figure 3-6: Inside the BiB Filter Wheel Enclosure**

#### **Grating/Mirror Turret:**

Each element in the turret is secured by four clips located in the corners, see Figure 3-7. The flat mirror, 150 lines/mm, and 600 lines/mm gratings are 12 X 12 X 7 mm in size. The 300 lines/mm grating is 10 X 10 X 3 mm in size. It has been installed in a spacer bracket which was then installed into the turret.



**Figure 3-7: InSb Grating/Mirror Turret**



If any problems arise with the installation of optical elements, do not hesitate to call Infrared Laboratories, Inc. at (520) 622-7074.

#### **4. Reassembly Instructions**

Much of the reassembly procedure is simply the steps in Section 2 in the reverse order. There are, however, some changes. An outline for reassembly follows, using the steps in Section 2 as a reference.

- (1) The aperture wheel and filter wheel enclosures for both the InSb and BiB should be reinstalled by reversing the instructions in Section 2.
- (2) Make sure all the electrical connectors are reinstalled (temperature sensors, heaters, array wiring, Home switches, etc.).
- (3) Reinstall the inner radiation shield lid using the forty (40) 4-40 socket head cap screws. Make sure to orient the lid such that the charcoal getter box is located opposite the windows.
- (4) Reinstall the outer radiation shield lid using the forty (4) 4-40 socket head caps screws. Align the 'W' on the shield lid with the window side of the dewar.
- (5) Inspect the o-ring on the bottom cover plate. Remove any debris and apply a thin layer of a good quality silicone vacuum grease. Infrared Laboratories uses Dow Corning 111.
- (6) Reinstall the bottom plate of the dewar using the sixteen (16) 8-32 socket head case screws provided. Make sure to line up the stamped number on the bottom plate with the one on the side of the dewar case.
- (7) Turn the dewar over so that it is resting on the bottom plate. Reinstall the valve using the four (4) 8-32 socket head cap screws provided.

Your dewar is now ready to use according to the instructions provided by Infrared Laboratories, Inc. If any problems arise with the unpacking or operation of your dewar system, do not hesitate to call Infrared Laboratories, Inc. at (520) 622-7074.

#### **5. Motor Drives**

There are four stepper motors mounted on the dewar. They control the InSb filter wheel, BiB filter wheel, InSb aperture wheel, and InSb grating turret. The motors have 200 mechanical steps per revolution, but can microstep at 52800 steps per revolution. The motor power supplies and indexers were not supplied with the dewar.

**Caution:** It is highly recommended that the user read the indexer manuals completely before operating the motors. Failure to do so may result in forcing the motor past a limit switch and breaking it.

## **6. Pumping the Guard Vacuum**

In order to prevent condensation and icing, as well as to ensure thermal isolation from the case, it is imperative that a dewar have an adequate guard vacuum. The interior of the dewar must be evacuated or the water vapor in the atmosphere, and also other substances with boiling points higher than that of nitrogen, will condense on all the cold parts of the dewar, including optics, detectors, filters, etc. Even if the dewar has enough of a vacuum to prevent condensation inside the dewar, just a small amount of contamination of the guard vacuum will allow heat transfer from the ~300 Kelvin case to the cold inner assemblies. This will result in seriously degraded cooling efficiency.

To pump a guard vacuum on a dewar requires a pump capable of pressures down to around 10 mTorr. Although a conventional mechanical pump is sufficient, a turbo pump would be preferable. A pressure gauge reading in the mTorr range is also essential.

- (1) Attach the dewar to the pump with a section of rubber hose or an Ultra-Torr fitting. Make sure that the vacuum valve on the dewar is closed.
- (2) Turn on the mechanical pump and open the pump valve to pump out the hose attached to the dewar. Allow the pressure gauge to stabilize before proceeding to the next step.
- (3) SLOWLY open the dewar vacuum valve. Watch the pressure gauge carefully to see when the pressure jumps, indicating that the valve is starting to open. Continue to open the valve slowly enough so the pressure gauge does not jump wildly to atmospheric pressure. This slow pump-out is done to protect the contents of the dewar from pressure gradients which can cause damage to fragile filters, or cause the foil lining in the dewar to bulge out from the case and shield.
- (4) Once the dewar valve is fully open, allow the pump to evacuate the dewar to below 100 mTorr. This may take from a couple minutes to a few hours, depending on the size of the dewar and the amount of contamination inside the dewar. Heating the case with a heat gun may help drive off any residue of solvents, oils, or water still inside the dewar.
- (5) Turn on the turbo pump or valve the dewar onto a diffusion pump, if one is available. Make sure the pump's cold trap is filled with liquid nitrogen. If no turbo pump or diffusion pump is available, continue pumping with the

mechanical pump. An ideal guard vacuum is at or below 5 mTorr, but pressures below 15 mTorr are adequate.

- (6) Precool the dewar with liquid nitrogen according to the instructions in Section 5. While precooling, the operator may notice the pressure drop to below 1 mTorr. This is normal, and is due to the rapid removal of vapors within the dewar as they condense onto the cold precooling coils.

**Note:** It is recommended that the dewar be left on the diffusion pump during precooling. This dewar uses charcoal getter to absorb outgas materials and maintain a high vacuum, but the charcoal only becomes effective at temperatures below 150 K. For this reason, it is best to continue pumping until temperatures have fallen below 150 K.

Because the guard vacuum is so important, every Infrared Laboratories dewar is leak checked and cooled at the factory to ensure proper operation. However, if the dewar is disassembled by the operator, the potential exists that an O-ring may be contaminated or damaged. If a dewar does not pump down properly, it may have a leak.

A leak can be located by selectively squirting small amounts of acetone on the suspected joints on the dewar, i.e. the connectors, valve, bottom plate, while the dewar is on the mechanical pump. (Take care not to get acetone on fragile windows.) If a leaking spot is hit with acetone, the pressure gauge will jump slightly, then slowly return to where it was before. If an O-ring joint is suspected, careful removal and inspection may reveal a metal chip or a hair in the groove. Cleaning and regreasing of the O-ring and groove should solve this problem. A good quality silicone vacuum grease is recommended; Infrared Laboratories uses Dow Corning 111. Other leaks may not be as obvious.

If you have a persistent leak or other problem, do not hesitate to call Infrared Laboratories, Inc. at (520) 622-7074.

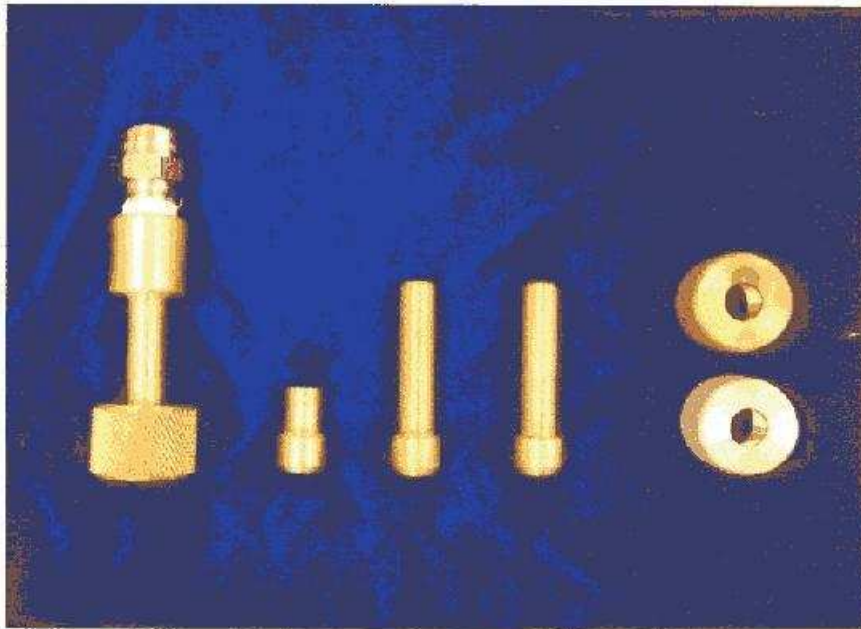
## **7. Liquid Nitrogen Precooling Instructions**

The procedure Infrared Laboratories used to cool the system was the following. A 160 liter liquid nitrogen storage tank was used with a supply pressure of ~22 psig. The valve of the supply tank was only partially opened to regulate the pressure.

Figure 7-1 shows the attachments used for filling and capping off the precooler ports. From left to right, the pressure relief valve, the plug, two fill tube extensions, and two knurled knobs.

- (1) Attach the fill tube extensions to each precooler port. See Figure 7-2.





**Figure 7-1: Precooler Port Attachments**

- (2) Attach a piece of 5/16 inch (3/32 inch thick wall) surgical tubing from the storage tank to the inlet precooler port. It does not matter which port is chosen for the inlet.



**Figure 7-2: Fill Tube Extension for LN<sub>2</sub> Precooler**

- (3) Attach the other fill tube extension to the vent port. It should also have a small piece of tubing attached to divert the nitrogen vent gas away from people and sensitive equipment.

- (4) Slowly open the supply valve. It may be necessary to use wire ties to securely fasten the tubing to the extensions.



**Figure 7-3: Fill Port Plug for LN<sub>2</sub> Precooler**

Feel the exhaust vent gas and increase the pressure until a steady flow is coming out. Allow the supply hose to freeze and watch the exhaust hose. If it also begins to freeze during the first half hour of precooling, then the supply pressure is too high.



**Figure 7-4: Pressure Relief Valve for LN<sub>2</sub> Precooler**

Once you have stopped using the precooler, the ports must be plugged with the proper hardware. Allow the hoses to thaw and remove the tube extensions from the



ports. Replace the extension with the supplied plug. Place the pressure relief valve over the other port and securely tighten the knurled nut. See Figures 7-3 & 7-4.

**Note:** It is very important that the pressure relief valve be placed on one of the ports. If both ports are plugged, an overpressure will occur inside the coil during warmup and the bellows could rupture. As the dewar begins to warm, liquid nitrogen trapped inside the coil vaporizes. If there is not an exhaust mechanism, the coil pressurizes tremendously and can explode. The pressure relief valve will open at about 3 psi of back pressure.

The temperature of the InSb stage, BiB stage, InSb Filter Wheel Enclosure, and cold work surface were monitored using a Lakeshore Model 330 Controller. The controller can only monitor two sensors at a time, so a switch box has been provided, see Figure 7-5. Refer to the 'Test Data' section of the manual for cooldown information.



**Figure 7-5: Temperature Controller with Accessories**

## **8. CTI 1050 Coldhead Operation**

The following procedure is used at Infrared Laboratories, Inc. to cryogenically test all hybrid systems (closed AND open cycle). This particular dewar is a hybrid of a liquid nitrogen precooling coil and a CTI 1050 coldhead. The benefit of such a system is no cryogen use after the initial cooldown. Certain precautions must be taken to safely cool the system to steady state.

- (1) Install the two helium compressor lines from the compressor to the 'Y' splitter manifolds using the 1 3/16 inch and 1 inch wrenches. Attach the small set of helium lines (the ones with the right angle at the ends) to each



of the 'Y' manifolds. This set of lines goes to the smaller M22 coldhead. Attach the remaining set of lines of the 'Y' manifolds and then to the M350 coldhead. Once the ends are securely tightened, plug the coldhead power cables into the coldheads. As the coldheads extract the Joule-mass from the system and the system gets cold, the nitrogen precooling coil will begin to cryopump if left open and unused. As a result, water moisture from the atmosphere will condense inside the coil. If the precooling coil is not used, cap off the ports using the brass plug over one port and tightening the knurled nut and placing the pressure relief valve over the other port.

**Caution:** The pressure relief valve is a critical component to the liquid nitrogen precooling coil. It must be placed on one of the ports whenever the precooler is not operational. If both ports are plugged, pressure will build up inside the coil as the dewar warms up and could rupture the bellows.

- (2) It is recommended that the precooling coil is purged with dry nitrogen gas before the ports are closed. This will prevent any atmospheric gas inside the coil from condensing as the dewar cools.



**Figure 8-1: CTI Helium Compressor with Lines**

- (3) The compressor can be turned on before, during, or after precooling with liquid nitrogen. It is recommended that the compressor is turned on first, then the coldhead power can be turned on. Similarly, when shutting the compressor off, turn the coldhead power off first, then the compressor. The Cooldown charts in the 'Test Data' section of the manual give a time frame for cooling the dewar with and without the use of the precooling coil.

Figure 8-1 shows the CTI compressor with the four ten foot 1.5" diameter helium lines and the two smaller 1" diameter helium lines. The small toolbox contains the wrenches necessary to install the lines and the precooler accessories.

## **9. Bake Out the InSb Array**

The InSb array is sensitive to atmospheric conditions. The material is hygroscopic and will absorb water molecules. The effect is visible on the array and is known as a 'picture frame' effect. On a clean, new array, the image will appear flat and uniform. As the array is exposed to atmosphere, a darker region around the edge of the array will begin to appear. Gradually over time, the effect will worsen, with the 'picture frame' slowly increasing in size toward the center. It is at the user's discretion to decide when the effect has become unacceptable. The following procedure describes the steps necessary to bake out the InSb array to remove some of the 'picture frame'.

- (1) With the InSb array mounted in the dewar, connect the dewar to a turbo pump or other pump. Allow the dewar to pump out for at least one day.
- (2) Completely open the Heat Switch.
- (3) The dewar must remain on a pump for the duration of the bake out. Begin to heat the InSb stage up to 330 K using the Lakeshore controller. There are three heater settings: low, medium, high. The low setting delivers 0.25 W, while the others deliver 2.5 and 25 W respectively. It is recommended to bake out the array for a minimum of two week.

## **10. SAFETY HAZARDS: Overpressure Buildup in Precooler Coil**

If an ice plug forms in the neck tube of the helium vessel, the result is extreme pressure buildup and eventually deformation or even rupture. A safety device/pumping attachment has been included with the dewar to reduce the possibility of this occurring. This device should be used even if the helium bath is not going to be pumped on.

Before attaching the pressure relief valve, check the teflon washer at the neck tube opening. If it shows signs of excessive wear, or no longer fits in the groove properly, replace it. The relief valve can then be inserted and screwed on hand tight, followed by another quarter to half turn with pliers.

When warming up the dewar, **DO NOT USE COMPRESSED AIR THROUGH THE COOLING COIL.** The air will condense and can form an ice plug in the coil. Pressure can build up behind the ice plug and rupture the coil. The cooling coil is not designed to aide in warming up the dewar.

#### **10. SAFETY HAZARDS: Guard Vacuum Failure**

If the guard vacuum fails, the result is a large quantity of room air being sucked into the vacuum space. This is indicated by an increase in all temperature sensors. As the dewar warms, the trapped room air expands and can cause damage to the internal components.

Guard vacuum failure should be dealt with by putting the dewar back on a vacuum pump and leaving it on while the dewar warms. The cause of the failure should then be investigated and corrected before cooling the dewar again.



# Acquisition Software

# InSb Acquisition Software

## User Manual

### 1. Introductory Overview

The InSb IR array covers the spectral band from 900 to 5000 nm. The InSb array is cooled to 35 Kelvin by a CTI refrigerator cold head to suppress dark current and thermal background. The 256x256 array of high QE photodiodes is scanned non-destructively at a rate of .25E6 pixels/second. This enables both over sampling to reduce read-noise and high frame rates.

The array is operated in 6 modes, which are described in Section 5. One mode provides continuous display of bright images at several frames per second while other modes acquire single images with pre-selected integration times from 0.05 second to >>100 second. The continuous display mode facilitates focusing and scanning the target. Automatic subtraction of background and fixed pattern noise is implemented before the images are displayed and saved to disk for further processing.

The InSb array from SBRC is the heart of the system. The San Diego State University/IR Labs array-controller, which is coupled to a PC, operates the array and acquires the 16-bit digital images.

### 2. Specifications

#### 2.1 Camera System

- a. Spectral range 900-5000 nm
- b. Science grade InSb IR-array; 256x256, 30  $\mu$ m pixels, 25 elec. read-noise rms
- c. Array controller; 4 channels, 16-bit, Fiber Optic to PCI-bus interface

#### 2.2 Software; IR Labs DOS program

- a. Sends commands to array controller
- b. Acquires images
- c. Displays, stores images

### 3. Functional Description of Hardware

#### 3 IR-array and controller electronics

The Hughes SBRC InSb array was chosen because of its spectral band (900-5000 nm), relatively high quantum efficiency, QE, and read-noise of about than 25 electrons. When operated at 35 K this InSb array displays dark current levels below 1 electron/sec

The array has 4 outputs, which read out alternate columns. By clocking the horizontal and vertical shift registers each output is simultaneously scanned, one pixel at a time. The dwell time on each pixel is 4 microsec, just long enough for the output voltage to reach equilibrium. A non-destructive sample is taken and the signal voltage, proportional to the integrated charge, is converted to a 16-bit integer that is sent to the data acquisition computer. Actually, all 4 samples are sent via the Fiber Optic to PCI bus to the computer memory in a period of less than 1 microsec—note, this implies that the outputs are operated in parallel. This is repeated until all 65,536 pixels are readout. A single readout of the array takes just over 65 millisec to complete. Consecutive resets of each pixel, carried out by a scan through the array with the reset line active, are used to remove accumulated charge and restore full bias voltage on the gate of the cooled PMos amplifier which is connected via indium bumps to each photo-diode.

This array operates well with a single reset frame followed by a single read. However, tests show some improvement with two consecutive reset frames that last 65 millisec each. Thus, 195 millisec is the minimum time to obtain an image. The resulting integration time, the time between when each pixel is reset and when it is read, is 65 millisec. Note that when the reset-read-read cycle is used the integration time is the time between the two non-destructive reads.

### 4. Functional Description of Software

The DOS program, *IREM2.exe*, is designed to control and operate the camera

\*\* There are 3 arguments to the INSB.exe

d:"xxxxxxx" for directory name where all new images will be stored.

s:"3 or 4" for screen size. 4 is default, 3 will give larger image display.

p:SDSU-IRL Password for DSP Menu.

When *INSB.exe* is loaded the Main Menu appears and unless given on the command line there is a prompt for the name of a sub-directory where the images will be stored. Commands are executed by hitting keys from the displayed menu and by typing inputs followed by <cr>. The first step is always to hit the Initialize key ( I ). This brings up the camera in its default, Mode-1, where the array is continuously being reset with no output.



There is a configuration file ( Cam.cfg ) that is an executable text file which can be changed in DOS which holds the current parameters, such as specific integration times, biases, etc..

The Main Menu contains all of the main commands, including all 6 camera modes, except for Mode-1 which is transparent and does not produce any output. The first item allows the default values for integration time in each mode to be changed. Note that the current integration time for each mode is displayed on the Menu. There are also commands for “darks” and “flats” and for inputting parameters that may be changed. The Sub-Menu is important for additional commands that will be needed, as described below. The Sub-Menu, ( **DSP** ), should never be used unless instructed to do so by IR Labs. They are included only for system installation and trouble-shooting. The exit command leaves the camera running in Mode-1. One reason for exiting the program is to remove the current “darks” and “flats” which are stored in memory. The program can be re-loaded at any time as long as the camera is running.

There is a particular setup of sub-directories for image storage. These sub-directories will require purging and editing if they are to be fully useful.

## **5. Operating Instructions**

### **5.1 Camera initialization**

This command must be issued each time the camera controller is either powered up or reset. It completes the task of setting up the proper operation of the array. It is not necessary to issue this command when the program is restarted and the controller has already been started. Note that the camera electronics must be powered on when the DOS program is loaded. Shutdown is optional but the program should be exited first. The preferred startup sequence is as follows:

1. Turn on the lower electronic Fiber Optic to PCI box.
2. Turn on the power to the camera controller.
3. Hit the reset button on the Fiber Optic to PCI Box
4. Start the DOS Program
5. Initialize the camera

### **5.2 Camera Modes**

#### **Model; Continuous Resets**

This is the default mode and it is invisible to the user. It consists of continuous resets carried out once the initialization is completed and when any of the imaging modes is completed. It prepares the array for the next operation and prevents undesired over-exposures. Note that over-exposing the array produces no permanent damage but does leave a persistent dark current effect that mimics a latent image if some pixels are saturated while others are not.

## Mode 2; "Video" Mode

Continuous reset-reset-integration-read. Each image is displayed along with mean pixel value and mean standard deviation from the mean. Video Mode is useful for focusing and scanning the target. Note that the display always auto-scales each image. This means that care must be taken to avoid saturation by reducing the illumination or the integration time or both. A feature common to all imaging modes is the automatic "dark" subtraction. This occurs once the appropriate "dark" image has been taken. This is a special form of "dark" where 4 consecutive images have been averaged to reduce noise in the "dark" image. Because the random noise in the "dark" is only half that in each image when the "dark" is subtracted only a small increase in random noise is added. The price for this benefit is the additional time spent taking each "dark". However, a "dark" will last for a long time so it is a good idea to take a "dark" early in each session and retake it only when degradation has become apparent or when the integration time has been changed.

\* Fastest Frame Rate = 4 Hz.

## Mode 3; Single image with 2 reads

Here a single image is displayed and saved to disk. The camera performs a double reset, a short pause, the first read, integration and finally a second read. The integration time has been set previously or the default value is used. There are two reasons for the two reads: (i) lower noise can be obtained by elimination of kTC noise associated with reset and (ii) all artifacts that are common to both reads are removed.

## Mode 4 Single image with 20 reads

As in Mode 3 the result is a single image. The 20 reads are used to reduce the read-noise from about 35 electrons with 2 reads to about 15 electrons with 20. The automated algorithm is to take 10 reads following the reset and 10 more reads following the integration. The first read in each set of 10 is discarded and the remaining 9 reads are averaged. Then the subtraction occurs to produce the final image. Mode 4 is the most sensitive mode and should always be used for integration times longer than 10 seconds since it will give the best result. Note that there is still some residual glow in the corners which originates from the shift registers. This glow subtracts out well when a "dark" has been taken and very little noise has been added. **Please Note** that this mode was first implemented for the PICNIC array and at this time is not functioning properly for the InSb.

## Mode 5; Accumulate

This mode is designed to produce images of thermal scenes where the photon rate is very high and where only very small temperature differences over relatively small areas are to be measured. The integration time is short, depending on the target temperature and which objective is used. A predetermined number of frames is selected for each block. Each frame consists of a reset-reset-integration-read. All frames in a block are

accumulated and averaged. Block1 is taken with the chip powered off. Block 2 is taken with the chip powered on. Block3 is taken with the chip powered off. Block1 and Block3 are averaged and subtracted from Block2. This results in a single image which is displayed. In general this sequence will be repeated many times so that each new image is added to the sum of all previous images. This results in a gradually improved signal-to-noise so that after several minutes very small temperature gradients can be seen in the displayed image. Once an adequate image is displayed the process can be terminated by an additional keystroke and the final image is saved to disk. **Please Note** that this mode was first implemented for the PICNIC array and at this time is not functioning properly for the InSb.

#### Mode 6, ( 1 Frame of Video )

Mode 6 is used for imaging thermal scenes where it is desirable to record the total emission from the target. A single reset-reset-read frame is taken. Integration times can be as short as 0.050 seconds. Provision is made for taking a "flat" using a smooth black surface that is ideally near and below the same temperature as the target. When the "flat" has been recorded it will be divided into each new image and the result will be multiplied by the mean of the new image. (Note that when no "flat" has yet been taken then each image is simply divided by a frame with all pixels set to unity.) This procedure flattens each image so that variations in pixel response or systematic variations in optical transmission are normalized out of the final image. **Please Note** that this mode was first implemented for the PICNIC array and at this time is not functioning properly for the InSb.

## 6. Appendices

### 6.1 Nominal array parameters

Format	256x256
Pixel size	30 $\mu\text{m}$ x 30 $\mu\text{m}$
Outputs	4
Spectral band	900 to 5000 nm
Max QE	0.92 e-/ph. at 1250 nm
Max dark current	1 e-/second
Lowest av. read-noise	25 e-
Max bad pixels	1900
Full well cap.	360,000 per bias volt



# **BiB Acquisition Software**

## **User Manual**

### **1. Introductory Overview**

The Rockwell BiB IR array covers the spectral band from 2000 to 28000 nm. The BIB array is cooled to 6-10 Kelvin by a CTI refrigerator cold head to suppress dark current and thermal background. The 128x128 array of high QE photodiodes is destructively scanned at a rate of 1E6 pixels/second. This enables both over sampling to reduce read-noise and very high frame rates.

The array is operated in 1 mode, which is described in Section 5. One mode provides both a continuous display of bright images at several frames per second while the same mode is also used to acquire a single image with pre-selected integration times from 0.001 second to >>100 second. The continuous display mode facilitates focusing and scanning the target. Automatic subtraction of background and fixed pattern noise is implemented before the images are displayed and saved to disk for further processing.

The BIB array from Rockwell is the heart of the system. The San Diego State University/IR Labs array-controller, which is coupled to a PC, operates the array and acquires the 16-bit digital images.

### **2. Specifications**

#### **2.1 Camera System**

- a. Spectral range 2000-28000 nm
- b. Science grade BIB IR-array; 128x128, 75  $\mu\text{m}$  pixels, <1300 elec. read-noise rms
- c. Array controller; 16 channels, 16-bit, Fiber Optic to PCI-bus interface

#### **2.2 Software; IR Labs DOS program**

- a. Sends commands to array controller
- b. Acquires images
- c. Displays, stores images

### 3. Functional Description of Hardware

#### 3.1 IR-array and controller electronics

The Rockwell BIB array was chosen because of its spectral band (2000-28000 nm) and relatively high quantum efficiency, QE. When operated at 6 K this BIB array displays dark current levels from 65 to 65000 e-/sec dependent upon bias.

The array has 16 outputs, which read out in a 2x8 block format. By clocking the horizontal and vertical shift registers each output, and block, is simultaneously scanned, one pixel at a time. The dwell time on each pixel is 1 microsec, just long enough for the output voltage to reach equilibrium. A destructive sample is taken and the signal voltage, proportional to the integrated charge, is converted to a 16-bit integer that is sent to the data acquisition computer. Actually, all 16 samples are sent via the Fiber Optic to PCI bus to the computer memory in a period of less than 1 microsec—note, this implies that the outputs are operated in parallel. This is repeated until all 16,384 pixels are readout. A single readout of the array takes just over 1 millisc to complete.

This array operates well with a single reset frame followed by a single read. The resulting integration time, the time between when each pixel is reset and when it is read, is an integral part of the clocking pattern and is user adjustable.

### 4. Functional Description of Software

The DOS program, *BIB.exe*, is designed to control and operate the camera.

\*\* There are 3 arguments to the *BIB.exe*

d:"xxxxxxx" for directory name where all new images will be stored.

s:"3 or 4" for screen size. 4 is default, 3 will give larger image display.

p:SDSU-IRL Password for DSP Menu.

There is also several flags which can be set to test various parts of the controller and software. "*BIB -?*" will provide a short help description of the command line arguments and flags.

When *BIB.exe* is loaded the Main Menu appears and unless given on the command line there is a prompt for the name of a sub-directory where the images will be stored. Commands are executed by hitting keys from the displayed menu and by typing inputs followed by <cr>. The first step is always to hit the Initialize key ( P ). This brings up the camera in its default, Mode-1, where the array is continuously being read out and clocked but no conversions are taking place, hence no output.

There is a configuration file ( *Cam.cfg* ) that is an executable text file which can be changed in DOS which holds the current parameters, such as specific integration times, biases, output offsets, etc..

The Main Menu contains all of the main commands. The first item allows the default values for integration time to be changed, the units are milliseconds. Note that the current integration time for each mode is displayed on the Menu. There are also commands for “darks” and sub menus for bias control and output line offset control. The Sub-Menu is important for additional commands that will be needed, as described below. The Sub-Menu, ( **DSP** ), should never be used unless instructed to do so by IR Labs. They are included only for system installation and trouble-shooting. The exit command leaves the camera running in Mode-1. The program can be re-loaded at any time as long as the camera is running.

There is a particular setup of sub-directories for image storage. These sub-directories will require purging and editing if they are to be fully useful.

## **5. Operating Instructions**

### **5.1 Camera initialization**

This command must be issued each time the camera controller is either powered up or reset. It completes the task of setting up the proper operation of the array. It is not necessary to issue this command when the program is restarted and the controller has already been started. Note that the camera electronics must be powered on when the DOS program is loaded. Shutdown is optional but the program should be exited first. The preferred startup sequence is as follows:

1. Turn on the lower electronic Fiber Optic to PCI box.
2. Turn on the power to the camera controller.
3. Hit the reset button on the Fiber Optic to PCI Box
4. Start the DOS Program
5. Initialize the camera

### **5.2 Camera Modes**

#### **Mode 2; “Video” Mode**

Continuous reset-integration-read. Each image is displayed along with mean pixel value and mean standard deviation from the mean. Video Mode is useful for focusing and scanning the target. Note that the display always auto-scales each image. This means that care must be taken to avoid saturation by reducing the illumination or the integration time or both. A feature common to all imaging modes is the automatic “dark” subtraction. This occurs once the appropriate “dark” image has been taken.

#### **Mode 3; Single image with 2 reads**



Here a single image is displayed and saved to disk. The camera performs a reset, an integration time and a read. The integration time has been set previously or the default value is used.

## 6. Appendices

### 6. Nominal array parameters

Format	128x128	
Pixel size	75 $\mu\text{m}$ x 75 $\mu\text{m}$	
Outputs	16	
Spectral band	2000 to 28000 nm	
Max dark current	65 e-/second	$1.7 \times 10^7 \text{ e}^-/\text{s}$
Lowest av. read-noise	< 1300 e- rms	
Charge Capacity	> 20,000,000 e	

# **InSb Focal Plane Array Specifications**

Hex co

Assembly # 41939

Detector# NI930726-27-C1

DATE PREPARED 05/29/97

Readout# 463-1-19-C3

ITEM	SPECIFICATION	MEASURED	TEST CONDITIONS*
Dark Current (35K)	<sup>2</sup> 40.0 aA	0.208 aA	ZILCH BB; 20.0 -2.0 sec
Read Noise (Low Doped)	<sup>2</sup> ? e-	34.28 e-	ZILCH BB; 1.0 sec
Q.E. (1.7 $\mu$ m )	<sup>3</sup> 80 %	81.5%	400K-300K; 0.5 sec
NEP Operability(1s; )	<sup>3</sup> 99 %	99.9%	400K-300Ksig/ZILCHnoise;1
NEP (1 sec)	<sup>2</sup> 2.5 E-17 W	0.333 E-17 W	400K-300Ksig/ZILCHnoise;1

\* All tests (unless otherwise noted) at: 35K FPA temperature, 100mV reverse detector bias, N/A V optimum gate bias, and using 2.45 $\mu$ m to 2.53 $\mu$ m (FWHM transmission) 2DFPA optical tube and pinhole aperture.

QUANTUM EFFICIENCY  
SCALED FROM 0 TO 100%

DARK CURRENT (at right)  
SCALED FROM -5.0 TO 10.0 atto Amps



## **CRC 463 ARRAY CALCULATIONS**

### **1. List of Definitions:**

Ne = Noise in electron volts

Vn = Noise Voltage in Micro Volts RMS zilch back ground

AVSF = Source Follower Gain

Idark = Dark Current In Atto Amps.

Vdark = Dark Current In Volts

BUK = Bucket Capacity

### **2. Constants:**

T1=integration time used for dark current measurement= 18 sec = 20-2 sec

T2=integration time used for 400K-300K signal measurement = 0.5 sec

Qdiff=irradiance used for 400K-300K signal measurement

Qdiff=Q400K-Q293K = 3.78 E +09 ph/(cm<sup>2</sup> sec)

Ad = optical area of a single detector = 8.1E-6 cm<sup>2</sup>

C = total capacitance (low doped) = 6.00 E-14 farads

Vd = detector reverse bias = 0.1V to 0.6V

q = elementary charge = 1.60 E-19 coulombs

### **3. Formulas:**

BUK (Vd) = Vd \* C/q <--- Theoretical Prediction

Ne = Vn \* C/(q \* AVSF)

Idark (50K) = C \* Idark signal/(T1 \* AVSF)

QE (400K-300K) = 100\*C\*(400K-300K signal)/(AVSF\*Qdiff\*T2\*q\*Ad)

NEP (1s;293K) = (Vn/400K-300Ksignal)\*H300K\*Ad/(1s/T2)

NEP (1s;400K-300KsigZILCHnoise) Operability = NEP number of pixels considered/65536(total pixels)

Assembly #41939

Test Operator Mike SmithDate Prepared 05/29/97

<u>Item</u>	<u>Reverse Detector Bias Voltages</u>				<u>Test Conditions*/Notes</u>
	<u>0 mV</u>	<u>100 mV</u>	<u>300 mV</u>	<u>600 mV</u>	
DRO Gain	632				Zilch BB; 0.50 s
Dark Current (aA)	0.208	0.414	34.55		Zilch BB; 20.0 -2.0 sec
Raw Signal (mV)	21.30	23.40	25.09		400K-300K; 0.50 sec
Noise (mV)	0.057	0.056	0.103		Zilch BB; 1.0 sec,MCS
NEP@1 sec (1E-17watts)	0.333	0.299	0.507		400K-300Ksig/ZILCHnoise; 1.0 sec
Net Signal (mV)	33.69	37.01	39.69		400K-300K; 0.50 sec
Q.E. @1.7 $\mu$ m (%)	81.56	89.63	96.11		400K-300K; 0.50 sec
Read Noise (e-)	34.28	33.79	68.74		Zilch BB; 1.0 msec
NEP Operability (%)	99.9	99.9	99.4		400K-300Ksig/ZILCHnoise; 1.0 sec
@1 sec (#)	65512	65503	65179		
Capacitance (pf)	---0.060-----				Low Doped InSb; C is actually a function of V

All tests (unless otherwise noted) at: 35K FPA temperature, 0 to 600 mV reverse detector bias, and using 2.45 $\mu$ m to 2.53 $\mu$ m (FWHM transmission) 2DFPA optical tube and pinhole aperture. Tested using CTS timing.

The CRC 463 array is tested in a 68 pin Hansen Dewar without inboard electronics. The dewar consist of a cold cap and light tube combination which houses the limiting aperture and spectral band pass filter, a cold radiation cap, and a outer vacuum shroud which hold a Germanium 2" X 0.156" non-A.R. coated window with a flat band pass of 47% from 1.8 um to approximately 14 um. Because the limiting aperture is considered pin hole in size, the radiometric calculations assume the black body distance to the FPA is that of the limiting aperture to the FPA. Additionally, the back ground temperature is assumed to be the ambient temperature viewed through the germanium window, which was not held rigidly stable and controlled only by the laboratory air conditioning. A 2.4% variation is possible.

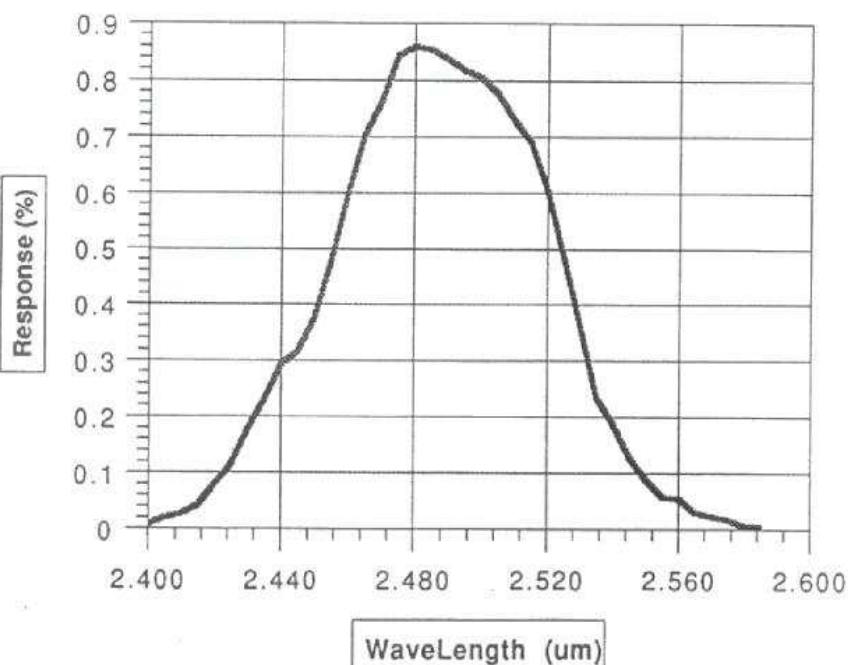
## **RADIOMETRIC TESTING PARAMETERS**

<b>PARAMETER</b>	<b>VALUE</b>	<b>UNITS</b>
<b>Q BACKGROUND</b>		
Temperature	300K	Kelvins
Flux	1.98E+07	Ph /cm2 /sec.
Watts	1.58E-12	Watts /cm2
Limiting Cold Aperture	0.0285	Inches
FPA To Aperture Distance	2.14	Inches
f #	75.44	
<b>Q SIGNAL</b>		
Temperature	400K	Kelvins
Flux	3.82E+09	Ph /cm2 /sec
Watts	3.04E-10	Watts /cm2
Limiting Cold Aperture	0.0285	Inches
FPA To Aperture Distance	2.14	Inches
FOV Attenuation	4.39E-05	

## **N-02518-6 BAND PASS FILTER DATA POINTS**

<b>Wavelength (um)</b>	<b>Transmission (%)</b>
2.390	0.003
2.395	0.005
2.400	0.008
2.405	0.0195
2.410	0.026
2.415	0.041
2.420	0.079
2.425	0.114
2.430	0.177
2.435	0.231
2.440	0.292
2.445	0.316
2.450	0.373
2.455	0.477
2.460	0.598
2.465	0.701
2.470	0.763
2.475	0.843
2.480	0.858
2.485	0.853
2.490	0.835
2.495	0.816
2.500	0.804
2.505	0.774
2.510	0.727
2.515	0.69
2.520	0.604
2.525	0.485
2.530	0.363
2.535	0.233
2.540	0.186
2.545	0.127
2.550	0.088
2.555	0.057
2.560	0.053
2.565	0.029
2.570	0.022
2.575	0.016
2.580	0.005
2.585	0.004

**N-02518-6 BAND PASS**





# Leakage Current, SCA #41939

Part # 2DFPA CRC-463

Serial # SCA #41939

Operator: Michael S Smith

Version: VMS 5.4-3, IFPATS 1 V1.0.0

VDDUC=-3.1; V3=-2.3; VGG=-1.5; VSS=GND; VDDOUT=-1.0

Aperture: 0, DC flux: 3.140E+07, AC flux: 0.000E+00 ph/(cm<sup>2</sup> sec)

VDET bias: -0.100 volts

Tint:0.5000 sec, Gain:-100.0, Frames: 10, Temp: 35K, 2DFPA Dewar

Output# 1

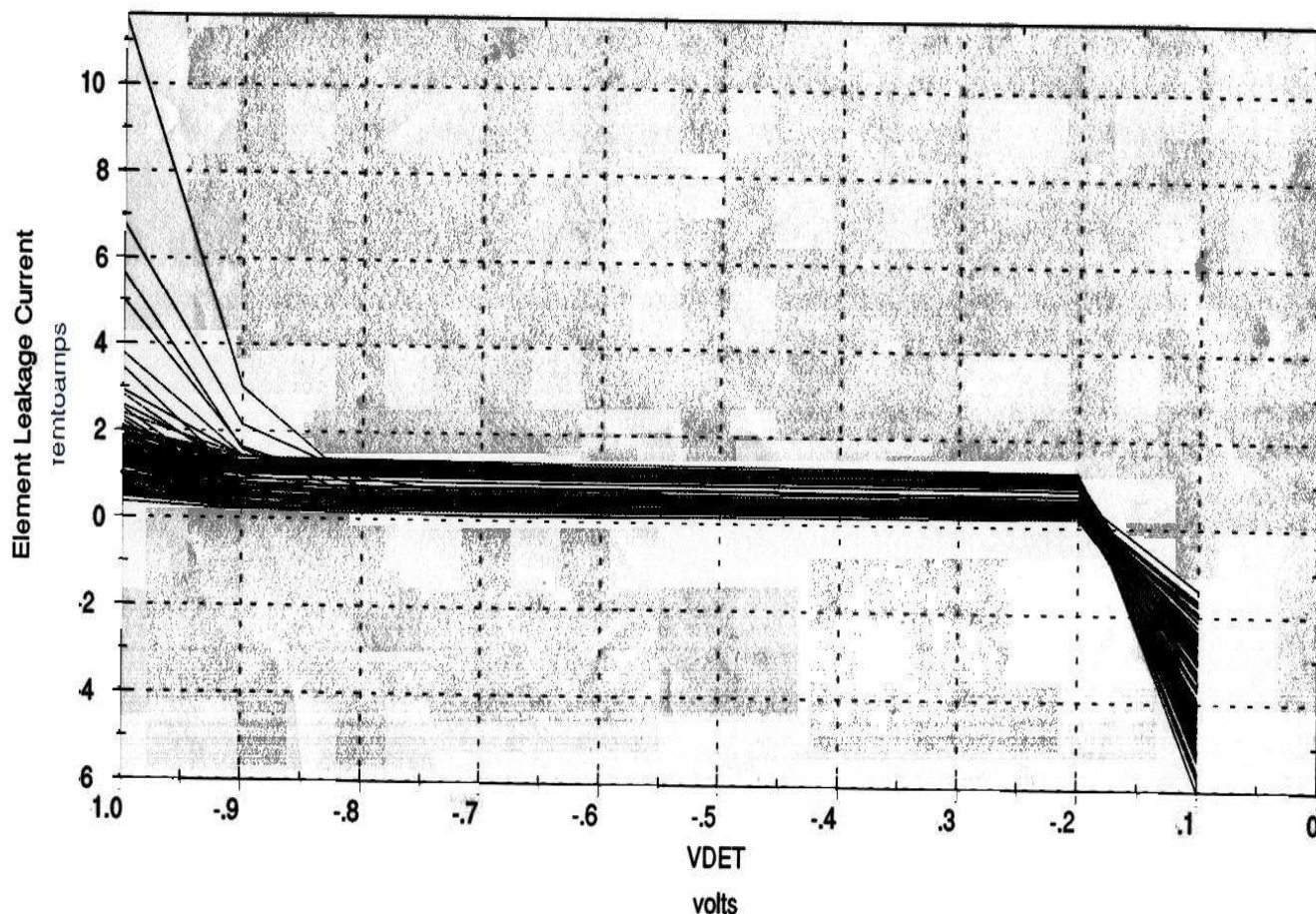
Register # 436

Secondary acquisition # 36

Date acquired: 28-MAY-1997 11:33:16.51

Date printed: 28-MAY-1997 11:38:25.01

2DATA:FPA\_41939\_DARK.REGS



James Garrett

**Test Condition Clock and Bias Parameters**  
**FPA#41939**

DC VOLTAGES			CLOCKS	LOW	HIGH
Vdd UC	- 3.1	-3.28	Ø SYNC S	-3.0	-6.0
Vgg	- 1.5	-1.5	Ø 1S	-3.0	-7.0
V3	- 2.3	-2.3	Ø 2S	-3.0	-7.0
Vdet	-2.8 to -2.2	-2.78	Ø SYNC F	-3.0	-6.0
Det Bias	0 to -0.6	-0.5	Ø 1F	-2.0	-7.0
Vgate	N/A		Ø 2F	-2.0	-7.0
Vdd Out	-1.0	-1.02	Ø RST	-3.2	-5.0
Vss	Gnd.				
Vsub	Gnd.				

↑ Ajustado 26/junio/2003. L.G

\*Detector reverse bias is zero at approximately 300 mV rev bias due to charge dumping in the device. Therefore, a 100mV reverse det bias will read Vdet=-2.70V.

\*Det Bias= Vdduc-Vdet

\*Adjust clocks Ø1S,Ø2S,Ø1F,Ø2F and ØRST for most uniform output.

offsets  
 Canal 1 3000  
 modified → 2 2100  
 3  
 4  
 no se pueden modificar

## TABLE OF CONTENTS

<u>PAGE</u>	<u>ITEM</u>	<u>BB TEMP</u>	<u>DET REV</u> <u>BIAS</u>	<u>GATE</u> <u>BIAS</u>	<u>INTEGRATION</u> <u>TIME</u>	<u>FPA</u> <u>TEMP</u>
1	DRO GAIN	ZILCH	0.0 mV	N/A	0.50 msec	35K
2	Dark Current(Amps)	ZILCH	100 mV	N/A	20.0-2.00 sec	35K
3	Dark Current Map	ZILCH	100 mV	N/A	20.0-2.00 sec	35K
4	Raw Signal(Volts)	400K-293K	100 mV	N/A	0.50 sec	35K
5	Noise(Volts)	ZILCH	100 mV	N/A	0.50 sec	35K
6	NEP@ 1 sec(watts)	400K-293K	100 mV	N/A	0.50 sec	35K
7	Opperability MAP	400K-293K	100 mV	N/A	0.50 sec	35K
8	Net Signal(Volts)	400K-293K	100 mV	N/A	0.50 sec	35K
9	Q.E.(%)	400K-293K	100 mV	N/A	0.50 sec	35K
10	Q.E. Map	400K-293K	100 mV	N/A	0.50 sec	35K
11	Dark Current(Amps)	ZILCH	300 mV	N/A	20.0-2.00 sec	35K
12	Raw Signal(Volts)	400K-293K	300 mV	N/A	0.50 sec	35K
13	Noise(Volts)	ZILCH	300 mV	N/A	0.50 sec	35K
14	NEP@ 1 sec(watts)	400K-293K	300 mV	N/A	0.50 sec	35K
15	Opperability MAP	400K-293K	300 mV	N/A	0.50 sec	35K
16	Net Signal(Volts)	400K-293K	300 mV	N/A	0.50 sec	35K
17	Q.E.(%)	400K-293K	300 mV	N/A	0.50 sec	35K
18	Dark Current(Amps)	ZILCH	600 mV	N/A	20.0-2.00 sec	35K
19	Raw Signal(Volts)	400K-293K	600 mV	N/A	0.50 sec	35K
20	Noise(Volts)	ZILCH	600 mV	N/A	0.50 sec	35K
21	NEP@ 1 sec(watts)	400K-293K	600 mV	N/A	0.50 sec	35K
22	OpperabilityMAP	400K-293K	600 mV	N/A	0.50 sec	35K
23	Net Signal(Volts)	400K-293K	600 mV	N/A	0.50 sec	35K
24	Q.E.(%)	400K-293K	600 mV	N/A	0.50 sec	35K
25	Read Noise (e-)	ZILCH	100 mV	N/A	0.50 sec	35K
26	Read Noise (e-)	ZILCH	300 mV	N/A	0.50 sec	35K
27	Read Noise (e-)	ZILCH	600 mV	N/A	0.50 sec	35K



# **BiB Focal Plane Array Specifications**

**Device Description and Operation Guide**  
**for the**  
**Boeing 128x128 HF16 Hybrid Focal Plane Array**



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***Revised November 9, 1998***

## 1.0 PURPOSE

This document provides a general overview of the Boeing 128x128 HF16 hybrid Focal Plane Array (FPA) and information on device operation. The topics include a description of the hybrid FPA, multiplexer pixel organization, package pin-out, dc bias lines and input clock waveforms, integration time control feature, pixel output waveform, temperature sensor, and continuity validation. The purpose of this document is to furnish users of the HF16 array with configuration information and operating requirements. Details relating to device performance and characteristics are specific to different supporting contracts, and as such are not covered by this document.

## **2.0 HYBRID FPA DESCRIPTION AND PACKAGE CONFIGURATION**

The HF16 ("HF" denotes High Flux, and "16" identifies the number of output lines) is a high-performance infrared hybrid focal plane array suitable for moderate-to-high photon flux infrared astronomy and aerospace applications. The device consists of a back illuminated Si:As BIB detector (128x128 elements with  $75 \times 75 \mu\text{m}^2$  pixel size) mated via indium columns to a matching multiplexer. The Si:As BIB is a wide infrared band (2-28  $\mu\text{m}$ ), high fidelity detector that operates at temperatures at or below 12K. The multiplexer is a direct readout device designed for operation at deep cryogenic temperatures. Each detector element (pixel) is connected to an input cell circuit via the indium column. Each input cell has an integration capacitor that is discharged through the respective detector element during the course of an integration period, and the current through the detector will depend on incident photon flux, detector bias, and temperature. Each integration capacitor is sequentially reset across the array, and the time that it takes to cycle from the end of one reset to the beginning of the next for a pixel is defined as the integration time. The multiplexer accesses the pixels in a "rolling read" fashion, in which the voltage on a given integration capacitor at the end of the integration period is read onto an output bus through a source follower amplifier circuit. More detail on the output configuration and readout is provided below.

The multiplexer has 16 separate output lines, where pixels are read out in a sequential manner. The outputs are linked to 2x8 blocks of pixels in the spatial arrangement shown in Figure 1. Block 1 (written as BL1 in the figure) contains pixel number      of each output, Block 2 contains



pixel number 2 of each output, etc. The output configuration within a block of pixels is shown in Figure 1. For each output line, at the beginning of a frame readout cycle, the corresponding pixel from Block 1 is read, then Block 2, etc. up to Block 1024. Therefore, an entire frame readout for each output line consists of 1024 pixels. This spatial arrangement enables each output to read pixels distributed over the entire array area. Blocks 1 to 16 (the first 16 pixels on each output) form the left-most two columns of array pixels (as viewing the packaged hybrid FPA with the output bond pads on the left). Blocks 17 to 32 form the next two columns of array pixels, etc.

Pixels are read out in a sequential manner as described above. The reset operation will now be explained. Reset occurs on a half-column length basis. Immediately after the eighth block of a given set of two columns is read, all the pixels of those eight blocks are simultaneously reset. Similarly, immediately after the sixteenth block of a given set of two columns is read, all the pixels of the ninth through sixteenth blocks from those two columns are simultaneously reset. This results in slightly different integration times for the pixels within a given column. On a given output, the first pixel read out of a column will integrate for  $7 \times T_{\text{pix}}$  ( $T_{\text{pix}}$  = pixel access time = frame time/1024) less than the eighth pixel read out of that column, and similarly the ninth pixel read out of a column will integrate for  $7 \times T_{\text{pix}}$  less than the sixteenth pixel read out of that column. This will cause a slight difference in the pixel output value for pixels along a column, but in most cases this difference is insignificant. For example, in the conventional integration mode, the total integration time for the first pixel read out of a given column will be 0.7% less ( $7/1024$ ) than the eighth pixel read out from that column. These differences can become more significant if the integration time control feature is used. Integration time control is described in a later section.

The HF16 hybrid FPA is mounted in a 68 pin leadless chip carrier (LCC). The LCC used here is fabricated by Kyocera Corporation (P/N PB-C87700-A). The pin-to-pin spacing for this type of 68 pin LCC is standard in the industry. The hybrid FPA is mounted to the LCC floor with the use of a sliver filled epoxy, allowing for both good electrical contact between the multiplexer substrate and LCC floor (the common ground point), as well as good thermal contact. The multiplexer pads of the hybrid FPA are wire bonded to the LCC pins using 1 mil aluminum wire. The pin-out arrangement is diagramed in Figure 2. The 16 wires that connect to the bus bars

mounted next to the multiplexer go to the 16 output drivers. This approach reduces the number of needed LCC pins, since the output drivers possess the same bias requirement. The pin functions and biases are covered in the next section.

### **3.0 DC LINES AND INPUT CLOCK WAVEFORMS**

Package pin numbers, multiplexer pad names, nominal voltages and approximate currents are listed in Table 1 for operation at or below a temperature of 12 K. The bias voltages and currents shown in Table 1 reflect the highest pixel rate advertised for the HF16, which is 4.2 MHz (240 nsec pixel access time). This corresponds to a frame time of 246  $\mu$ sec (4.1 kHz frame rate). Current in the digital circuitry, as well as the required load and drive currents, will be less at lower pixel rates, and this would result in decreased power dissipation.

The pads labeled VDD\_HS and VSS\_HS denote the connections that provide the main power to the multiplexer, as well as to the rails for the high-speed logic (vertical shift register). Pads VDD\_RST, VSS\_RST, VDD\_SEL, and VSS\_SEL are the high and low rail supply lines for the reset and select (also referred to as access in this document) MOSFETs. VDD\_DIG and VSS\_DIG are the rails for the low-speed logic (horizontal shift register). Pad VTUB\_DIG provides connection to the N-wells in the multiplexer, as well as the high rail of the gate protection circuitry, and is required to be set higher than all other multiplexer bias supplies.

Figure 3 is a schematic of the analog circuitry. Pads CUR\_GL, CUR\_GU, CUR\_SL and CUR\_SU are the supply lines for the gates and sources of the internal bus load MOSFETs. The "U" and "L" at the end of these names indicate which set of outputs these pads serve. CUR\_GL and CUR\_SL serve the lower eight outputs (1-8), while CUR\_GU and CUR\_SU serve the upper eight outputs (9-16). A separate load MOSFET exists on each bus. To reduce the number of power supplies used, CUR\_GL and CUR\_GU can be connected together, as well as CUR\_SL and CUR\_SU, since the bias requirements are the same. Assuming this is done, we can use the shorthand CUR\_G for both sets of gates and CUR\_S for both sets of sources (note that the current through CUR\_S will be twice that of the separate connections). The following comments apply to these terms together or separately. For optimal operation, the values of CUR\_S and CUR\_G should

be set to allow for adequate pixel settling time for a given pixel rate. The values listed in Table 1 are appropriate for a 4.2 MHz pixel rate. For slower rates, CUR\_S should be kept the same, and CUR\_G should be reduced to no lower than the point where pixel settling time is sacrificed. This will reduce the multiplexer power dissipation. VACC is the drain connection of the in-cell source follower MOSFETs, and is the drain current path from the sources of the internal bus load MOSFETs.

Pads labeled Out 1 through Out 16 are the sources of the 16 output driver MOSFETs. These need to be connected to a load (constant current source, JFET, or resistor load) that provides the necessary drive current. The required current depends on the pixel rate and capacitive loading on the outputs. 1 mA per output is sufficient to drive the 4.2 MHz pixel rate and approximately 70 pF of output line capacitance. Again, this current can be reduced at lower rates in order to decrease multiplexer power dissipation. One can experimentally determine the minimum output driver current value by observing the pixel output stream from a given output, and reducing the current to no lower than the point where pixel settling time is sacrificed. The drains of the 16 output driver MOSFETs are connected to two pins, VDD1-8 and VDD9-16 (each output MOSFET drain gets connected through the bus bar described earlier). These pins can be connected to a common supply, since the bias requirements are the same.

VRST, DET\_SUB, and VDI are bias lines in the unit cell. VRST supplies the reset voltage to the unit cell integration capacitor. VRST is enabled by the shift registers/reset logic, and the integration capacitor of a given unit cell is reset each frame after the pixel read access (the previous section explained the reset operation in more detail) and is held to this reset value for two pixel periods in the conventional mode of operation. The reset is held longer when the integration time control feature is used, and this is described in the next section. VDI connects to the gate of the direct-injection MOSFET within the unit cells. The drain of this FET connects to the integration capacitor, while the source is connected via indium bumping techniques to the top contact of the detector. The function of the direct injection MOSFET is to isolate the detector top contact from the voltage on the integration capacitor, so that the detector is not debiased while the capacitor discharges during the integration period. DET\_SUB is the connection to the buried (backside)



contact of the detector array. The detector bias is equal to the difference between DET\_SUB and VDI minus the threshold voltage of the direct-injection MOSFET, which is approximately 1 V at deep cryogenic temperatures (<12 K). Therefore, given the VDI bias listed in Table 1 and setting DET\_SUB to 3.5 volts, the detector bias would be  $(VDI-1) - DET\_SUB = (6-1) - 3.5 = 1.5$  volts. DET\_GRD connects to the detector guard ring that runs around the perimeter of the 128x128 pixel detector array, and protects the outer pixel elements from field fringing.

Power supply filtering may be necessary on certain dc input lines. Multiplexer noise performance may suffer if power delivered to the following lines is noisy: VRST, VDI, DET\_SUB, VACC, CUR\_G, or CUR\_S. If low-pass filters are used on any of these lines, please be aware that the voltages and currents listed in Table 1 are specified for the input pads on the multiplexer. Therefore, if a filter is used and there is a bias drop, the supply voltage will need to be adjusted in order to deliver the specified voltages and currents to the device.

The input clock waveforms and their functional relationship to the multiplexer will now be discussed. A diagram of the input clock waveforms is shown in Figure 4. FST\_CLK is the fastest clock input to the multiplexer, and controls the high speed shift register (reading up a column). Pixels are read out sequentially onto their respective output lines with each change in state of this clock. LSYNC stands for line (column) synchronization, and this clock controls the slow speed shift register (shifts from one pair of columns to the next). Each change in state of LSYNC advances the readout to the next pair of columns. Within the time of an LSYNC state, 16 pixels are read up a given column pair on each output line per the 2x8 block spatial relationship described earlier via the fast register. FSYNC stands for frame synchronization, and cycles once each frame (initiates the first pixel access of a frame). For the conventional mode of operation, the FSYNC high state must be more than 32 pixel periods long, but less than 64 (this is what is reflected in Figure 4). For the mode of operation in which the integration time control feature is employed, the FSYNC pulse needs to be extended. The integration time control technique is described in the following section. The actual timing presented in Figure 4 represents the highest readout rate (frame rate of 4.1 kHz, pixel rate of 4.2 MHz). To extend the frame time, increase the FST\_CLK

period as well as that of the other clocks, maintaining the cycle relationships shown in Figure 4 between all of the clocks.

#### **4.0 INTEGRATION TIME CONTROL**

The HF16 array includes an integration time control feature, which enables the unit cells to integrate for time periods anywhere from 1/32 of the frame time up to the full frame time (less the time it takes to reset a pixel after the read). This feature is valuable for those situations in which very high photon fluxes must be accommodated, and the integration time must be decreased below the minimum specified frame time.

Integration time is increased via the integration time control feature by extending the FSYNC pulse length. For the maximum integration time within a given frame time, the FSYNC high state must last more than 32 pixel periods (i.e., 32 FST\_CLK state changes), but less than 64. This is what is illustrated in Figure 4. For each group of 32 more pixel periods that FSYNC is held high (a full LSYNC cycle), the integration time is reduced by this amount. Therefore, integration time can be reduced in increments of the LSYNC cycle time (32 pixel periods), up to a maximum reduction of 1/32 the frame time. Note that simply extending the FSYNC pulse in this manner is not the preferred method of decreasing the integration time within a given frame time, because pixel input cells are being hit with multiple reset pulses for this period following the time in which they are read, and this creates the potential to increase noise. The use of OVERRIDE eliminates the multiple reset pulses during the extended reset period. For the conventional mode of operation, OVERRIDE is set low (to ground). If OVERRIDE is set to 9.0 volts in conjunction with the extended FSYNC pulse, pixels will be held to a constant reset value after their read for the period of time in which the FSYNC pulse is extended (in multiples of LSYNC cycles). This is the recommended approach to using the integration time control feature.

#### **5.0 PIXEL OUTPUT WAVEFORM AND CHARGE CAPACITY**

Each output includes a stream of 1024 pixels per frame, read out from the array per the spatial arrangement previously described. Each pixel access places the integrated output voltage for that pixel onto the output bus. The reset occurs subsequent to the pixel access period, thus the pixel

reset level is not readable. This allows more time for pixel output settling, and results in a 4.2 MHz maximum pixel rate. The pixel output level for a zero detector bias, or a dark background with temperature less than or equal to 12 K at a given detector bias, is approximately 4.5 volts above ground. This is commonly referred to as the “quiescent” level. Increases in background flux, integration time, and/or detector bias will decrease the pixel output voltage level. This level drops because during integration, the input integration capacitance discharges after reset through the detector, decreasing the voltage on the capacitor, which is subsequently read out through the source follower circuit onto the output bus at the end of the integration period. The pixel signal is determined by subtracting one output level of interest from another, e.g., the pixel outputs are sampled and stored for a scene background, then the process is repeated without the scene, then the signal is obtained by differencing the results.

In order to validate multiplexer functionality prior to cooling down to the focal plane operating temperature, two bias levels need to be adjusted. The biases listed within Table 1 are for the focal plane operating at  $T < 12$  K at the fastest rate. At room temperature, a zero bias needs to be applied to the detectors, and CUR\_S should be adjusted to provide the specified current through CUR\_S (due to MOSFET threshold voltage difference between room and deep cryogenic temperatures). Actually, it is not absolutely necessary to change CUR\_S, since not having the appropriate load current is not an issue simply for a room temperature check. To apply a zero detector bias at room temperature, note that the formula to use in determining detector bias is different from what was presented in Section 3.0 (top of page 5). The threshold difference at room temperature requires that 0.7 volt be subtracted from VDI, rather than 1 volt, resulting in the relationship:  $\text{Detector bias} = (\text{VDI} - 0.7) - \text{DET\_SUB}$ . Therefore, to apply a zero detector bias at room temperature, set DET\_SUB to 5.3 volts. DET\_GRD will also need to be set to 5.3 volts. Under these conditions, the output level should be approximately 4.5 volts above ground, with no current observed across DET\_SUB. To verify the DET\_SUB connection, one needs to disconnect DET\_GRD, and apply a small bias to the detector. Setting DET\_SUB to 5.0 volts should be sufficient to see current across DET\_SUB and a drop in the output level. After this verification, remove power from the device, reconnect DET\_GRD, and set biases in preparation for operation at cryogenic temperature.



To translate pixel signal voltage or output noise voltage to number of electrons referred to the input, the following equation is needed:  $N = (C_{\text{eff}} * V_o) / e^-$ , where  $N$  is the number of electrons referred to the input,  $C_{\text{eff}}$  is the effective integration capacitance in farads,  $V_o$  is the output signal or noise in volts, and  $e^-$  is electron charge in coulombs. The effective integration capacitance is the actual capacitance divided by the source follower gain. For the HF16 array,  $C_{\text{eff}} = 1.7 \text{ pF}$ .

The maximum output voltage swing (full well) of the HF16 array is 2 volts. This corresponds to a pixel output level of approximately 2.5 volts above ground. Therefore, using the relationship in the previous paragraph, the full well input charge capacity is  $2.1 \times 10^7$  electrons. The device read noise for the 4.2 MHz pixel rate has been measured to be between 95 to 100  $\mu\text{V}$ -rms. Again, using the above relationship, this translates to approximately 1,050 noise electrons. For lower flux and therefore lower pixel rate applications, the noise will drop with a decrease in measurement bandwidth.

A 5.1 k $\Omega$ , carbon resistor is included in the LCC for temperature sensing. The resistor is bonded to the LCC floor with thermally conductive, electrically non-conductive material. The pin assignments for this resistor are provided in Table 1 as well as Figure 2. Table 2 provides temperature versus resistance values for this resistor.

## **6.0 CONTINUITY VALIDATION**

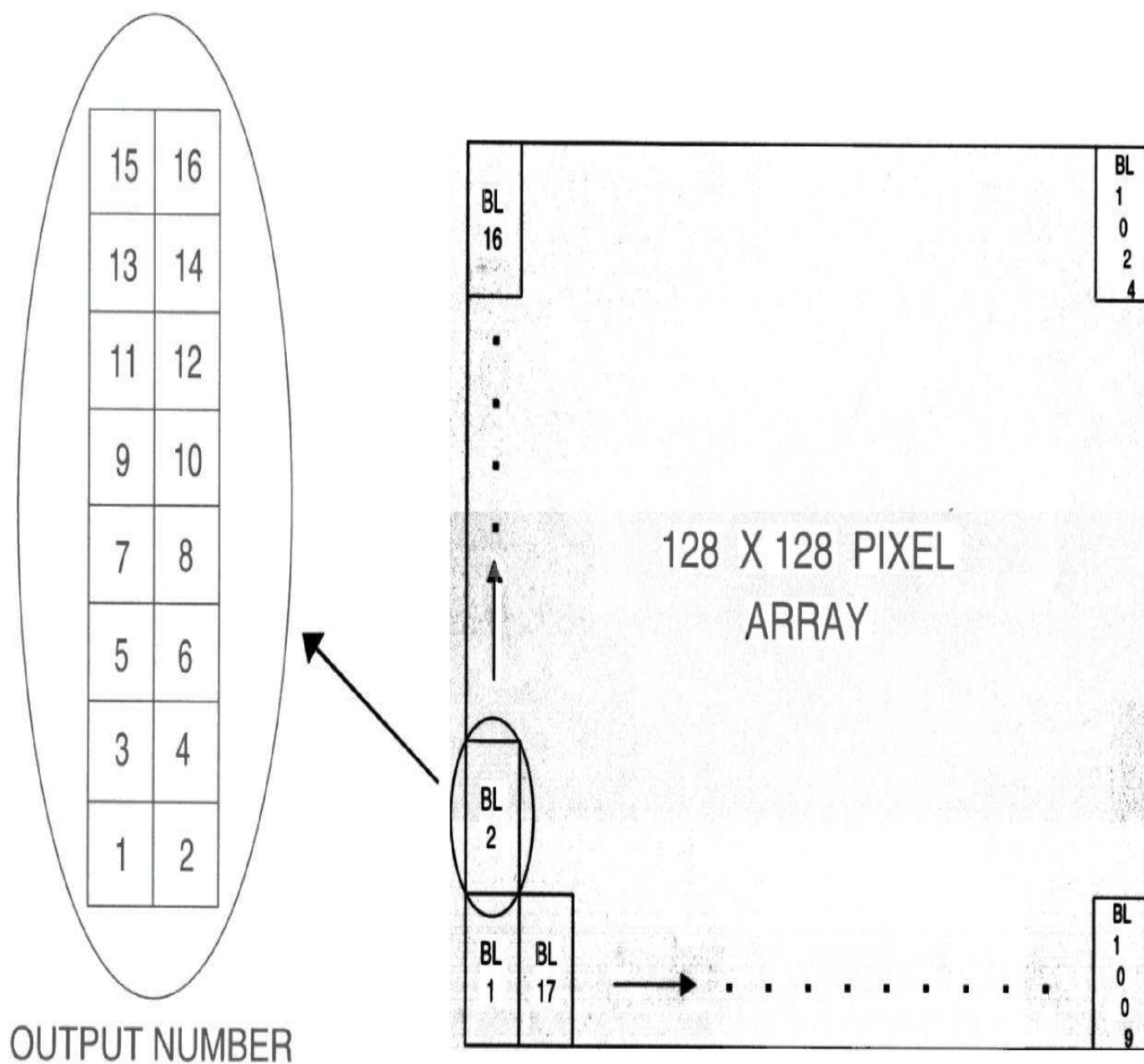
If a focal plane array is observed not to operate properly at room temperature, the operating currents should be checked for any out of range values as an initial step to investigating the problem. If this examination does not reveal anything obvious, then the suggested approach would be to perform an isolation (between each line and line to ground) and continuity (source input to socket pin on each line) validation. If there are no issues with the socket or cryostat, then a visual inspection should be performed on the packaged focal plane to check the wire bonds per the pin-out diagram. If operation is proper at room temperature, but not at the cryogenic operating temperature, the physical continuity check down to the socket pins can not be performed since the cryostat is secured. In this case, the semiconductor characteristics of the device inputs can be used to check

for opens or shorts (this technique can also be used at room temperature). The focal plane input lines are connected to contacts interfacing to either insulator (MOSFET gate), n-type material, or p-type material. The lines that are connected to gates also connect to gate protection circuitry (back-to-back diodes). Table 3 lists the I-V characteristic between given sets of lines. This information is used to check for any shorts or opens. To perform the validation, power to the focal plane array must be shut off, and supply input lines removed.

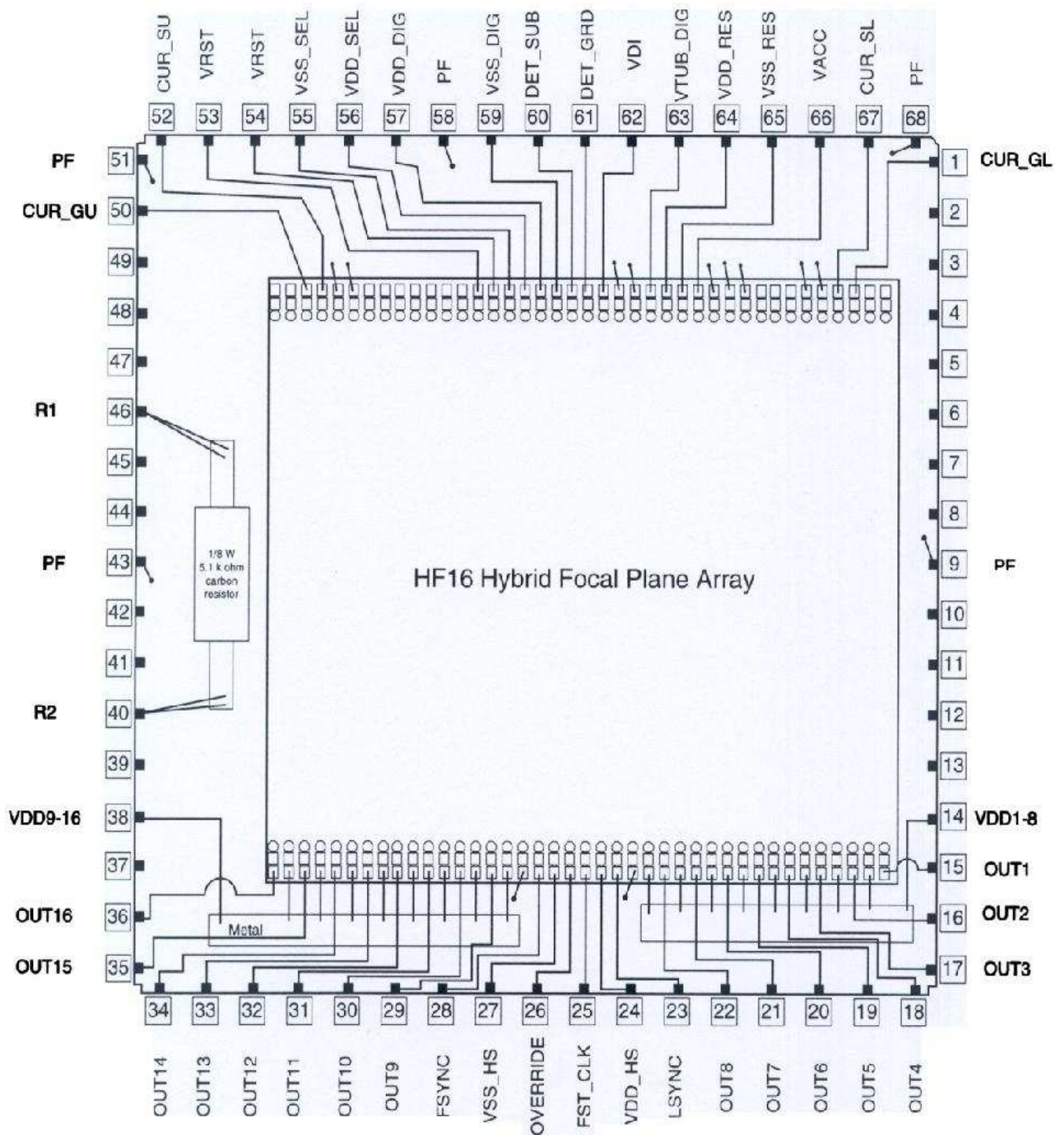
## **7.0 CUSTOMER SUPPORT**

The intent of this document is to provide users of the Boeing HF16 hybrid FPA with the necessary information to operate the array as well as a description of array configuration and parameters needed for applications. It is understood that the information contained within may not be able to address every question a user may have, and in such cases the user should not hesitate to get in touch with the appropriate Boeing contact. The level of support beyond that dealing with general device operation is defined by the specific contract.

FIGURE 1 - HF16 HYBRID FPA OUTPUT/PIXEL CONFIGURATION



**FIGURE 2**  
**HF16 HYBRID FPA PACKAGE PIN-OUT**





**TABLE 1****HF16 HYBRID FOCAL PLANE ARRAY****NOMINAL OPERATING VOLTAGES AND CURRENTS @ FRAME TIME = 246 $\mu$ sec (T<12K)**

PIN #	NAME	NOMINAL VOLTAGE (V)	APPROXIMATE CURRENT ( $\mu$ A)	FUNCTION
1	CUR_GL	4.0	0	Gate of internal bus load FET (lower half)
9	PF	Ground		Package floor (multiplexer substrate)
14	VDD 1-8	5.6	(1)	Drain of output driver FETs (outputs 1-8)
15-22	OUT1-OUT8		(1)	Source of output driver FETs (outputs 1-8)
23	LSYNC	9 high / 4 low		Line (column) sync clock - slow register
24	VDD_HS	9.0	350	High speed logic high rail
25	FST_CLK	9 high / 4 low		Fast clock - fast register
26	OVERRIDE	9 enable / ground disable		Enables extended reset when set high
27	VSS_HS	4.0	-350	High speed logic high rail
28	FSYNC	9 high / 4 low		Frame sync clock
29-36	OUT9-OUT16		(1)	Source of output driver FETs (outputs 9-16)
38	VDD9-16	5.6	(1)	Drain of output driver FETs (outputs 9-16)
40	TS1			One side of 5.1 kohm temperature sensor
46	TS2			Other side of 5.1 kohm temperature sensor
50	CUR_GU	4.0	0	Gate of internal bus load FET (upper half)
51	PF	Ground		Package floor (multiplexer substrate)
52	CUR_SU	2.45	-750	Source of internal bus load FET (upper half)
53,54	VRST	6.9	(2)	Reset voltage for input node
55	VSS_SEL	4.0	-75	Select low rail
56	VDD_SEL	9.0	75	Select high rail
57	VDD_DIG	9.0	20	Low speed logic high rail
58	PF	Ground		Package floor (multiplexer substrate)
59	VSS_DIG	4.0	-20	Low speed logic low rail
60	DET_GRD	5.0	(2)	Detector guard ring
61	DET_SUB	Vary for detector bias <sup>3</sup>	(2)	Detector substrate (Detector bias = 5V - DET_SUB)
62	VDI	6.0	0	Gate of direct injection FET
63	VTUB_DIG	9.5	0	Digital N-well
64	VDD_RES	9.0	30	Reset high rail
65	VSS_RES	4.0	-30	Reset low rail
66	VACC	6.0	1500	Drain of internal source follower
67	CUR_SL	2.45	-750	Source of internal bus load FET (lower half)
68	PF	Ground		Package floor (multiplexer substrate)

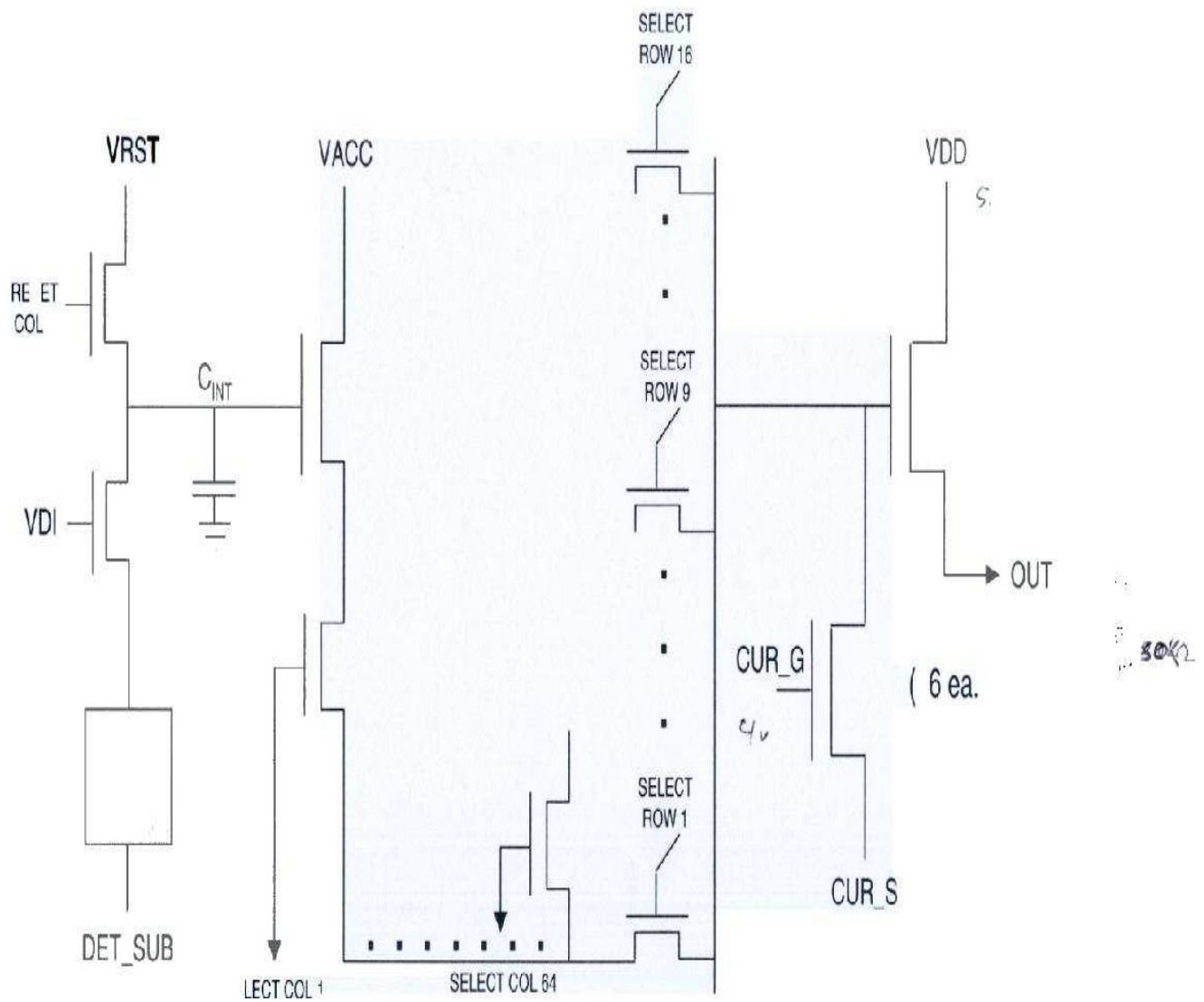
- Notes:**
- (1) The current depends on the output load and number of outputs connected. For the frame rate listed here, a 1 mA load needs to be connected to each output. The current will be equal to the sum of the number of outputs connected. The Boeing measurements only have one output connected at a time.
  - (2) Current on these lines will depend on flux and detector bias. VRST current will be nearly equal and opposite to DET\_SUB current (current through DET\_GRD represents the difference).

**General Notes:**

- Many of the logic lines with identical bias requirements can be connected together to conserve on the total number of power supplies required. This also holds true for the CUR\_S's and CUR\_G's
- Pins 9, 51, and 68 should have a very low impedance to system ground to minimize noise.

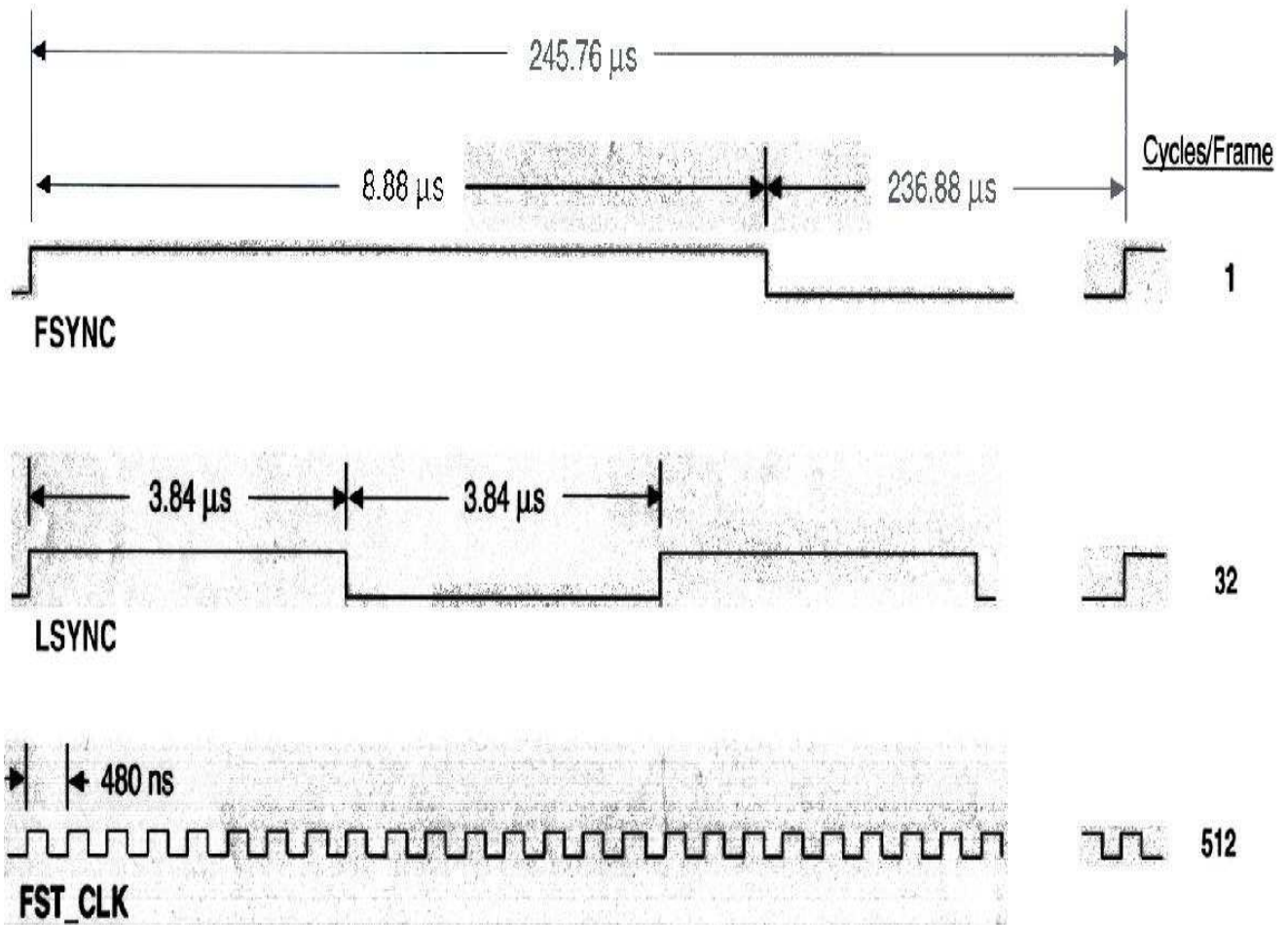
# FIGURE 3

## HF 6 ANALOG CIRCUIT SCHEMATIC



**FIGURE 4**

**HF16 Input Clock Waveforms**



**TABLE 2**  
**Temperature vs Resistance**  
**of Packaged Temp Sensor Resistor**

Temperature (K)	Resistance (K $\Omega$ )
4.3	358
4.5	311
4.6	291
4.7	273
4.8	257
4.9	242
5	228
6	140
7	96.5
8	73.5
9	59.2
10	49.7
11	43.0
12	38.2
13	34.6
14	31.6
15	29.0
16	26.6
18	23.1
20	20.9
22	19.0
23	18.4
24	17.7
26	16.7
27	16.2
28	15.9
29	15.5
30	15.2
31	14.8
32	14.5
33	14.2
34	13.9
35	13.7
36	13.5
38	13.0
39	12.8
40	12.6
44	12.0



**TABLE 3**

**Boeing 128x128 HF16 Hybrid Focal Plane Array  
I-V Characteristic Information in Support of Continuity Check**

<u>Bias Terminal</u>	<u>Common Terminal</u>	<u>I-V Characteristic</u>
VDD_DIG	VTUB_DIG	Forward Diode
VSS_DIG	PF*	Reverse Diode
VDD_HS	VTUB_DIG	Forward Diode
VSS_HS	PF*	Reverse Diode
VDD_RES	VTUB_DIG	Forward Diode
VSS_RES	PF*	Reverse Diode
VDD_SEL	VTUB_DIG	Forward Diode
VSS_SEL	PF*	Reverse Diode
VRST	PF*	Reverse Diode
DET_SUB	PF*	**
DET_GRD	PF*	**
VACC	PF*	Reverse Diode
CUR_S	PF*	Reverse Diode
CUR_G	PF*	Back-to-Back Diode
VDI	PF*	Back-to-Back Diode
VDD1-8, 9-16	PF*	Reverse Diode
VTUB_DIG	PF*	Reverse Diode
OVERRIDE	PF*	Back-to-Back Diode
FST_CLK	PF*	Back-to-Back Diode
LSYNC	PF*	Back-to-Back Diode
FSYNC	PF*	Back-to-Back Diode
OUT1-OUT16	PF*	Reverse Diode

\* PF is the package floor and multiplexer substrate contact, which is the common ground during focal plane operation.

\*\* This will be a reverse diode at room temperature, and open at cryogenic temperatures.

**General Notes:**

- For the Reverse Diode characteristics noted, a negative bias is swept on the bias terminal against the common terminal listed (n-diffusion within p-material).
- For the Forward Diode characteristics noted, a positive bias is swept on the bias terminal against the common terminal listed (p-diffusion within n-material).
- For the Back-to-Back Diode characteristics noted, a diode is observed for both polarities of the bias terminal (due to back-to-back gate protection diodes connected to these lines).
- Disconnect multiplexer input power and lines to the terminals while performing continuity tests.
- Current should not exceed 1 mA on any line while performing continuity tests.